DUAL BAND KRAMER

HARDWARE

INTERFACE DOCUMENT

1 REVISION HISTORY

Issue	Date	Purpose
REV 1.0	4/1/98	Kramer First Release
REV 1.1	8/10/98	General Editing
REV 1.2	8/14/98	General Editing
REV 1.3	8/20/98	Added IRQ Section, Hookswitch Change, Removed Proposed Matrix
REV 1.4	10/14/98	Added B+ Threshold data, Therm data for 38 deg., new audio gains, contrast control definition. Changed –5V_EN description, ONOFF1/2 power up sequence.
REV 1.5	10/29/98	Added default states for RTS/EXT_CHG_ENABLE, corrected line states. Added charger section. Added Added display power down sequence.

2 PURPOSE / INTRODUCTION

The purpose of this document is to list and define the supplies and interfaces for the International GSM/DCS Kramer cellular phone. The radio will bring to market the WCP (Wireless Communication Processor), GCAP II audio interface and power control IC as well as the air interface MAGIC IC.
At the time of market introduction The WCP core will run at 1.8V all the other ICs will run at 2.775V. A 1.8V version will evolve from the original design as soon as the interface ICs (SRAM, Flash ROM etc.) become available. This document is meant as a guide for the hardware and software implementation.

All signals are CMOS levels unless otherwise stated. Signals with a '*' in front of them are active low, all others are active high. CMOS levels are taken from the WCP signal specification, and are as follows (Vcc is defined as 2.7V):

*Vih:	0.7*Vcc to (Vcc+0.3Vdc)
*Vil:	(Vss-0.3Vdc) to 0.2*Vcc
*Voh:	(Vcc-0.2Vdc) to Vcc
*Vol:	0 to 0.4Vdc

3. GCAP II Hardware Overview

Global Control Audio Power II (GCAP II) is a power and audio management IC. It incorporates many of the functions of various different power and audio management ICs into one platform. Kramer will be using the 100 ball BGA package.

- Five programmable linear regulators (VSIM1, Ref, V1, V2, and V3) which provide all voltages for the logic IC's.
- Two Buck or Boost switching regulators (PWM#1 and PWM#2)
- Five audio amplifiers (A1 through A5) for driving the speaker, alert, and external audio or amplifying signals from the transceiver microphone, and external microphone
- One 13 bit linear audio CODEC for bringing in external digital audio data
- One 8 channel 8 bit A/D
- One PA high end regulator which is used to create ALRT_VCC for driving the alert and back light.
- One real time clock which is used for the sleep mode clock.
- A charger control circuit
- Turn on and turn off control circuits to properly control powering the transceiver.

3.1 Power Management

3.1.1 PGM0,1,2 Hardware Configuration

PGM0 and PGM1 alone determine the battery mode of GPAP II. This is necessary because the startup and shutdown voltages need to be available without processor intervention. The following shows the start-up configurations available.

PGM0	PGM1	Battery Mode	Switcher #1 Mode	Switcher #2 Mode
B+	0	3 cells	000 (Pass through)	000 (Pass through)
0	0	3 cells	110 (BOOST)	010 (2.2V BUCK)
B+	B+	4 cells	110 (BOOST)	100 (3.2VBUCK)
0	B+	5 cells	100 (3.2V BUCK)	010 (2.2V BUCK)

SWModeA and B Bit Definition

SWMode2	SWMode1	SWMode0	Output V	Mode
0	0	0	Pass thru	BUCK
0	0	1	1.875V	BUCK
0	1	0	2.20V	BUCK
0	1	1	2.775V	BUCK
1	0	0	3.20V	BUCK
1	0	1	3.80V	BUCK
1	1	0	5.60V	BOOST
1	1	1	Power down switcher	

At power-up, SWMode will be determined by PGM0 and PGM1.

At power-up PGM2 alone determines the output of V3. If PGM2 is connected to B+, V3 is 2.775V. If PGM2 is connected to ground, as in Kramer, V3 is 2.003V. No processor intervention is necessary.

3.1.2 V2 Linear Regulator

V2 is a programmable linear regulator. It is programmed through the SPI bus to outputs from 2.775V to 3.6V in 0.12V steps. For Kramer V2 is programmed to 2.775V. The regulator is supplied by B+ **Note: P1 Modulus B+ can not exceed 7.0V**. Future versions of GCAP II will support having V2 supplied by PA_DRV therefore the limit on B+ will change to 9.0V. This regulator is on whenever the radio is turned on. V2 is the supply for WhiteCap logic outputs, RAM, FLASH, and display.

3.1.3 V3 Linear Regulator

V3 is a programmable linear regulator with an output voltage which is determined by PGM2 at power-up. It is either 2.008V if PGM2 is connected to ground or 2.775V if PGM2 is connected to B+. After power-up V3 can be programmed through the SPI bus to voltages from 1.8V to 2.8V in 0.13V steps. For Kramer V3 is programmed to 1.8V. The regulator is supplied by B+ **Note: P1 Kramer B+ can not exceed 7.0V**. Future versions of GCAP II will support having V3 supplied by PA_DRV therefore the limit on B+ will change to 9.0V. V3 is the supply for the WhiteCap core (does not include logic output supply). For example, V3 supplies the ARM core, Clock amplifier, DSP Core, and input logic. For Ram 2 Whitecap V3 is programmed to 1.8V.

3.1.4 VSIM Regulator

VSIM is a programmable linear regulator. It is programmed through the SPI bus to either 5.0V or 3.0V. For Kramer VSIM is programmed dynamically to 5.0V. VSIM is supplied by V_BOOST1 and supplies the SIM card.

3.1.5 V1 Regulator

V1 is a programmable linear regulator. It is programmed through the SPI bus to either 5.0V or 2.775V. For Kramer V1 is programmed to 5.0V and is supplied by V_BOOST1 This regulator is on whenever the radio is turned on. V1 supplies the DSC bus.

3.1.6 V_BOOST1 Switcher Regulator

V_BOOST1 is a switching regulator. At power up pins PMG0 and PMG1 determine the mode of the switcher. For Kramer V_BOOST1 is programmed to 5.6V because PMG0 is shorted to B+ and PMG1 is shorted to ground. This regulator is on whenever the radio is turned on. V_BOOST1 supplies V1 and VSIM. The Boost regulator is PWM#2 for P1 Modulus **Note: P1 Kramer B+ can not exceed 7.0V.** Future designs of GCAP II will have PWM#1 as the boost regulator in 4 cell mode. Therefore the 7.0V limit on B+ will increase to 9.0V.

3.1.7 V_BUCK Switcher

V_BUCK is a switching regulator. At power up, pins PMG0 and PMG1 determine the mode of the switcher. For Kramer V_ BUCK is not used. The current GCAP II design uses PWM#1 as the Buck

regulator in 4 cell mode. This will change to PWM#2 in the future. Note: the max. input voltage on PWM#2 (PSCR2) is 7.0V.

3.1.8 SQ_OUT -5V Charge Pump Switcher

SQ_OUT is a square wave with a peak to peak voltage equal to VIN1-0.1V. It is used to create an unregulated charge pump voltage equal to -(VIN1-0.1V-2*VF_{diode}). For Kramer this output should be disabled.

3.1.9 PA_DRV Alert/Backlight Regulator

PA_DRV is a programmable linear regulator which drives an external P channel MOSFET. It is programmed by setting PA_B3-0 to one of 16 codes corresponding to an output of 2.6V to 7.00V incremented by 0.40V steps. Initially PA_DRV is off until set via SPI. For Kramer PA_DRV regulates ALRT_VCC to 3.0V (PA_B3-0=0001). This regulator is turned on and off by LS3_TX if PA_ON1 is enabled (high). PA_DRV powers the alert and backlights. Future GCAP IIs will have PA_DRV power up at 5.8V and only allow programming up to 7.0V. This way PA_DRV can supply V2IN and V3IN without exceeding the 7.0V maximum input.

3.2 Audio Management

3.2.1 Audio Output

3.2.1.1 A1 Earpiece Speaker Amplifier

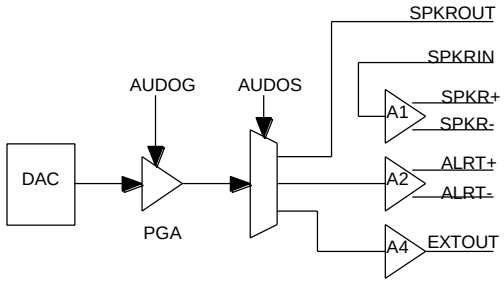
A1 is the transceiver earpiece speaker amplifier. It is powered by V2 and is driven through a multiplexer by the audio CODEC output. A1CTRL disables SPKR+ if high, but does not enable or disable SPKR-.

3.2.1.2 A2 Alert Amplifier

A2 is the alert amplifier. It is powered by ALRT_VCC and is driven through a multiplexer by the audio CODEC output.

3.2.1.3 A4 External Audio Output Amplifier

A4 is the external speaker amplifier. It is powered by V2 and is driven through a multiplexer by the audio CODEC output.



Above is a block diagram of the audio output section. Any one of three outputs can be selected. These outputs connect to the earpiece speaker amplifier, A1, the alert amplifier, A2, and the external audio out amplifier, A4. All outputs use the same converter so only one output is active at a time (unless A2ON is programmed high).The gain of the output can be selected in 5dB steps from -35dB to +0dB. This gain block is an analog system.

The Audio Output bits are programmed via SPI and they control the configuration of the output section. These bits select the gain, enable or disable the audio output, select or deselect dithering, and select or deselect the high pass output filter.

CODEC Output High Pass/Low Pass Filter

AUDOHPF	Description
0	Low pass filter only
1	Enables high pass filter with low pass filter

At this point in development high pass filter should be disabled.

Audio Output Bit Definition (all are R/W)

Name	# of Bits	Description
AUDOG	3	Audio Output Gain (-35dB to +0dB in 5dB steps)
AUDOS	2	Audio Output Select (A1, A2, A4, or no output)
ADITH	1	Audio Output Dither bit. Logic low enables dithering.
AUDOHPF	1	Audio Output High Pass Filter. Logic high enables the filter.

For Kramer the Audio Output bits for AUDOS, ADITH, and AUDOHPF should be set to all zeros. (This is the same as power-up default for AUDOS and ADITH. See 3.4.5 SPI Data Structure for addresses.) AUDOG should be set to all ones for lowest gain.

AUDOG Bit Definition

Bit	Description
AUDOG0	Logic high adds -5dB, logic low adds 0dB
AUDOG1	Logic high adds -10dB, logic low adds 0dB
AUDOG2	Logic high adds -20dB, logic low adds 0dB

AUDOS Bit Definition

AUDOS1	AUDOS0	Output Selected
0	0	None (to power off, CDC_EN =0 and AUDOS =00)
0	1	A1 (A1 powered up)
1	0	A2 (A2 powered up)
1	1	A4 (A4 powered up)

Audio Output Dither, ADITH

When the output dither bit, ADITH, is reset to a logic low, dithering is enabled. Dithering decorrelates the periodic modulator quantization noise of the output converter. If ADITH is set to a logic high, dithering is disabled.

3.2.2 Audio Input

3.2.2.1 A3 Transceiver Microphone Amplifier

A3 is the transceiver microphone amplifier. It is powered by V2 and, through a multiplexer, drives the audio CODEC input

3.2.2.2 A5 Aux Microphone Amplifier

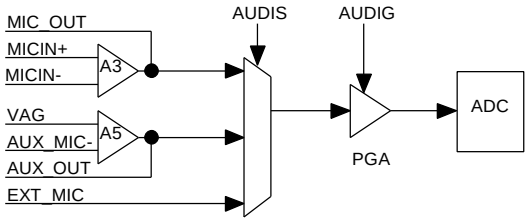
A5 is the AUX microphone amplifier. I t is powered by V2 and, through a multiplexer, drives the audio CODEC input

3.2.2.3 External Microphone Codec Input

This is an external microphone input without amplification and is used for the headset microphone. This input, through a multiplexer, drives the audio CODEC input

Below is a block diagram of the audio input section. Any one of three equivalent microphone inputs can be selected. These inputs are EXT_MIC, the output of the differential input microphone amplifier, A3 or, the output of the differential auxiliary microphone amplifier, A5. These three inputs are single ended with respect to VAG. Note that MICIN+ should be DC connected to VAG to avoid an offset relative to the A/D input. MIC_BIAS is derived from VAG for best noise performance. MB_CAP bypasses the gain from VAG to MIC_BIAS to keep the noise balanced.

MIC_BIAS is disabled if CDC_EN is low or if AUDIS is programmed to 00.



Following the input stage and multiplexer is a selectable gain stage and 30kHz low-pass antialiasing filter. This lowpass filter may be designed to whatever order is needed to insure that aliased components are not present in the output. The gain of the selectable gain stage can be selected in 1dB steps from -7dB to +8dB. Depending on the design of the A/D converter the output of the antialiasing filter may be clamped to keep from overdriving the A/D converter.

The audio input A/D converter converts the incoming signal to 13-bit 2's compliment linear PCM words at an 8 or 8.1 kHz rate. Following the A/D converter, the signal is digitally filtered, low-pass and selectable high-pass.

The digital filter characteristics are shown below. The filter characteristics are the same for both input and output except for the high pass function. (Note that all filter frequencies increase by 8.1/8.0 if DCLK is selected to generate FSYNC = 8.1kHz)

CODEC Input High Pass/Low Pass Filter

AUDIHPF	Description
0	Low pass filter only
1	Enables high pass filter with low pass filter

The audio input bits control the configuration of the input section. These bits select the gain, enable or disable the input, select between the EXT_MIC, A5 amplifier output, or A3 amplifier output, and select or deselect the high pass input filter. Also, these bits can select a loopback mode that takes the digital output of the input A/D converter, and loops it directly back to the D/A output section for testing.

Audio Input Bit Definition (all are R/W)

Name	# of Bits	Description
AUDIG	4	Audio Input Gain (-7dB to +8dB in 1dB steps)
AUDIS	2	Audio Input Select (EXT_MIC, AUX_MIC, or A3)
AUDIHPF	1	Audio Input High Pass Filter. Logic high enables the filter.
ALM	1	Audio Loopback Mode. Logic high enables loopback.

For Kramer the Audio Input bits for AUDIG, AUDIS, AUDIHPF, and ALM should be set to all zeros. (This is the same as power-up default for AUDIS and ALM. See 3.4.5 SPI Data Structure for addresses.)

AUDIG Bit Definition

Bit	Description
AUDIG0	Logic high adds 0dB, logic low adds -1dB
AUDIG1	Logic high adds 0dB, logic low adds -2dB
AUDIG2	Logic high adds 0dB, logic low adds -4dB
AUDIG3	Logic high adds 8dB, logic low adds 0dB

AUDIS Bit Definition

AUDIS1	AUDIS0	Input Selected
0	0	None (input section and MIC_BIAS powered off)
0	1	MICIN (and powers up A3)
1	0	AUX_MIC (and powers up A5)
1	1	EXT_MIC

Audio Loopback Mode, ALM

When audio loopback mode, ALM, is set to a logic high, the output of the A/D converter is looped back to the input of the D/A converter. In this mode the performance of the CODEC is degraded to that of a second order modulator. Loopback mode is used for testing. When ALM is reset to logic low, loopback is disabled.

3.2.3 Audio Paths

The Following table shows the required settings for the different audio configurations supported by Kramer.

	GCAP II SPI			**GPIO**
Configuration	**AUDOS1,0**	**AUDIS1,0**	**A1CTRL**	**BOOM_EN**
Internal Audio	01b	01b	L	H
Boom Headset	01b	10b	H	L

3.2.4 Gain Lineups

The Following tables define the audio output gains for the various Kramer audio configurations.

KRAMER AUDIO GAIN TABLE **9/24/98**

Handsfree - Default
Table(Regular Voice)

BIC Vol. Cntrl	Hardware Vol. Cntrl	Spkr Multiplier	Sdtone Multiplier	Speaker Attenuation	Sdtone Attenuation	Total Spkr Gain	Total Sdtone Gain	Sidetone Lev
0	**0**	0	**0**	7FFF	**7FFF**	-20.0	0.0	**XX**
1	**0**	0	**0**	7FFF	**7FFF**	-15.0	0.0	**XX**
2	**0**	0	**0**	7FFF	**7FFF**	-10.0	0.0	**XX**
3	**0**	0	**0**	7FFF	**7FFF**	-5.0	0.0	**XX**
4	**0**	0	**0**	7FFF	**7FFF**	0.0	0.0	**XX**
5	**0**	0	**0**	7FFF	**7FFF**	5.0	0.0	**XX**
6	**0**	0	**0**	7FFF	**7FFF**	10.0	0.0	**XX**
7	**0**	0	**0**	7FFF	**7FFF**	15.0	0.0	**XX**

Handsfree - Alert Table

BIC Vol. Cntrl	Hardware Vol. Cntrl	Spkr Multiplier	Sdtone Multiplier	Speaker Attenuation	Sdtone Attenuation	Total Spkr Gain	Total Sdtone Gain	Sidetone Lev
0	**0**	0	**0**	7FFF	**7FFF**	-20.0	0.0	**XX**
1	**0**	0	**0**	7FFF	**7FFF**	-15.0	0.0	**XX**
2	**0**	0	**0**	7FFF	**7FFF**	-10.0	0.0	**XX**
3	**0**	0	**0**	7FFF	**7FFF**	-5.0	0.0	**XX**
4	**0**	0	**0**	7FFF	**7FFF**	0.0	0.0	**XX**
5	**0**	0	**0**	7FFF	**7FFF**	5.0	0.0	**XX**
6	**0**	0	**0**	7FFF	**7FFF**	10.0	0.0	**XX**
7	**0**	0	**0**	7FFF	**7FFF**	15.0	0.0	**XX**

Handsfree - Tones
Table(DTMF Tones)

BIC Vol. Cntrl	Hardware Vol. Cntrl	Spkr Multiplier	Spkr/Sdtone Mult.	Speaker Attenuation	Sdtone Attenuation	Total Spkr Gain	Total Sdtone Gain	Sidetone Lev
0	**0**	0	**0**	4800	**7FFF**	-25.0	0.0	**XX**
1	**0**	0	**0**	4800	**7FFF**	-20.0	0.0	**XX**
2	**0**	0	**0**	4800	**7FFF**	-15.0	0.0	**XX**
3	**0**	0	**0**	4800	**7FFF**	-10.0	0.0	**XX**
4	**0**	0	**0**	4800	**7FFF**	-5.0	0.0	**XX**
5	**0**	0	**0**	4800	**7FFF**	0.0	0.0	**XX**
6	**0**	0	**0**	4800	**7FFF**	5.0	0.0	**XX**
7	**0**	0	**0**	4800	**7FFF**	10.0	0.0	**XX**

HandSet - Default
Table(Regular Voice)

BIC Vol. Cntrl	GCAPII Vol. Cntrl	Spkr Multiplier	Spkr/Sdtone Mult.	Speaker Attenuation	Sdtone Attenuation	Total Spkr Gain	Total Sdtone Gain	Sidetone Lev
3	4	0	2	7200	65AB	-21.0	10.0	-11.0
4	3	0	2	5A7E	47FA	-18.0	7.0	-11.0
4	3	0	1	7FFF	6567	-15.0	4.0	-11.0
5	2	0	1	65AB	47FA	-12.0	1.0	-11.0
6	1	0	0	50C2	65AB	-9.0	-2.0	-11.0
6	1	0	0	7200	47FA	-6.0	-5.0	-11.0
7	0	0	0	5A7E	32FA	-3.0	-8.0	-11.0
7	0	0	0	7FFF	2412	0.0	-11.0	-11.0

HandSet - Default Boosted
Table(Alert)

BIC Vol. Cntrl	GCAPII Vol. Cntrl	Spkr Multiplier	Spkr/Sdtone Mult.	Speaker Attenuation	Sdtone Attenuation	Total Spkr Gain	Total Sdtone Gain	Sidetone Lev
0	3	0	**0**	5A7E	**7FFF**	-18.0	0.0	**XX**
0	3	0	**0**	7FFF	**7FFF**	-15.0	0.0	**XX**
0	2	0	**0**	65AB	**7FFF**	-12.0	0.0	**XX**
0	1	0	**0**	50C2	**7FFF**	-9.0	0.0	**XX**
0	1	0	**0**	7200	**7FFF**	-6.0	0.0	**XX**
0	0	0	**0**	5A7E	**7FFF**	-3.0	0.0	**XX**
0	0	0	**0**	7FFF	**7FFF**	0.0	0.0	**XX**
0	0	1	**0**	7FFF	**7FFF**	6.0	0.0	**XX**

HandSet - Tones Table(In Call -Tones)

BIC Vol. Cntrl	GCAPII Vol. Cntrl	Spkr Multiplier	Spkr/Sdtone Mult.	Speaker Attenuation	Sdtone Attenuation	Total Spkr Gain	Total Sdtone Gain	Sidetone Lev
3	4	0	3	4000	5A7E	-26.0	15.0	-11.0
3	4	0	2	5A7E	7FFF	-23.0	12.0	-11.0
3	4	0	2	7FFF	5A7E	-20.0	9.0	-11.0
4	3	0	1	65AB	7FFF	-17.0	6.0	-11.0
5	2	0	1	50C2	5A7E	-14.0	3.0	-11.0
5	2	0	0	7200	7FFF	-11.0	0.0	-11.0
6	1	0	0	5A7E	5A7E	-8.0	-3.0	-11.0
6	1	0	0	7FFF	4000	-5.0	-6.0	-11.0

HandSet - Tones Boosted Table(Out of Call - Tones)

BIC Vol. Cntrl	GCAPII Vol. Cntrl	Spkr Multiplier	Spkr/Sdtone Mult.	Speaker Attenuation	Sdtone Attenuation	Total Spkr Gain	Total Sdtone Gain	Sidetone Lev
0	4	0	**0**	7200	**7FFF**	-21.0	0.0	**XX**
0	3	0	**0**	5A7E	**7FFF**	-18.0	0.0	**XX**
0	3	0	**0**	7FFF	**7FFF**	-15.0	0.0	**XX**
0	2	0	**0**	65AB	**7FFF**	-12.0	0.0	**XX**
0	1	0	**0**	50C2	**7FFF**	-9.0	0.0	**XX**
0	1	0	**0**	7200	**7FFF**	-6.0	0.0	**XX**
0	0	0	**0**	5A7E	**7FFF**	-3.0	0.0	**XX**
0	0	0	**0**	7FFF	**7FFF**	0.0	0.0	**XX**

Boom Headset - Default Table(Regular Voice)

BIC Vol. Cntrl	GCAPII Vol. Cntrl	Spkr Multiplier	Spkr/Sdtone Mult.	Speaker Attenuation	Sdtone Attenuation	Total Spkr Gain	Total Sdtone Gain	Sidetone Lev
0	4	0	1	7200	7FFF	-21.0	6.0	-15.0
0	3	0	1	5A7E	5A7E	-18.0	3.0	-15.0
0	3	0	0	7FFF	7FFF	-15.0	0.0	-15.0
0	2	0	0	65AB	5A7E	-12.0	-3.0	-15.0
0	1	0	0	50C2	4000	-9.0	-6.0	-15.0
0	1	0	0	7200	2D6A	-6.0	-9.0	-15.0
0	0	0	0	5A7E	2026	-3.0	-12.0	-15.0
0	0	0	0	7FFF	16C2	0.0	-15.0	-15.0

Boom Headset - Tones Table(In Call - Tones) **(Out of call same Level)**

BIC Vol. Cntrl	GCAPII Vol. Cntrl	Spkr Multiplier	Spkr/Sdtone Mult.	Speaker Attenuation	Sdtone Attenuation	Total Spkr Gain	Total Sdtone Gain	Sidetone Lev
0	4	0	3	1449	7FFF	-36.0	18.0	-18.0
0	4	0	3	1CA7	7FFF	-33.0	18.0	-15.0
0	4	0	3	2879	5A7E	-30.0	15.0	-15.0
0	4	0	2	392C	7FFF	-27.0	12.0	-15.0
0	4	0	2	50C2	5A7E	-24.0	9.0	-15.0
0	4	0	1	7200	7FFF	-21.0	6.0	-15.0
0	3	0	1	5A7E	5A7E	-18.0	3.0	-15.0
0	3	0	0	7FFF	7FFF	-15.0	0.0	-15.0

GCAPII Decimal	AUDOG2 Bit5	AUDOG1 Bit6	AUDOG0 Bit7	H/W Attenuation
0	0	0	0	0
1	0	0	1	-5
2	0	1	0	-10
3	0	1	1	-15
4	1	0	0	-20
5	1	0	1	-25
6	1	1	0	-30
7	1	1	1	-35

3.3 WhiteCap/GCAP II Audio Codec I/F

3.3.1 Audio CODEC Characteristics

The Audio CODEC uses the SPI interface for control and uses a four wire serial interface for transfer of the digital audio to the DSP. The clock input to the CODEC is a direct coupled sinusoidal signal from CLK_IN (or may be a CMOS square wave from CLK_IN with a duty cycle of 40/60 or better) which should always be on unless the CODEC core is reset or powered down.

If CDC_EN is low and AD_EN is low then the slicer on CLK_IN is disabled. CLK_IN is divided within GCAP II to generate the DCLK signal. DCLK is divided within GCAP II to generate the FSYNC signal. The input clock and division rates are selected by the CODEC control bits as defined below. In all cases CLK_IN, FSYNC, and DCLK are derived from the same reference.

If DCLK0-2 is set to 000 then FSYNC and DCLK are accepted as inputs from the external device connected to the serial interface. The IC will power up to this default state.

CODEC Control Bit Definition (All are R/W except as noted.)

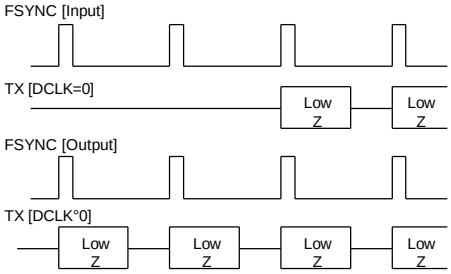
Name	# of Bits	Description
DCLK	3	Selects the CODEC clock input and output frequencies
CDBYP	1	A logic high routes the ADC input to the DAC output and powers down the CODEC core. In this mode CLK_IN does not need to be present, and CDC_EN needs to be programmed high.
CLK_INV	1	A logic high inverts the serial interface clock (IN or OUT)
FS_INV	1	A logic high inverts the frame sync (IN or OUT)
DF_RESET	1	DF_RESET resets the digital filter in the CODEC. (Write only)
CDC_EN	1	A logic high enables the CODEC, logic low puts the CODEC in battery save mode. Power up default is 0.

For Kramer the CODEC bits described above should be set to power-up default state: all bits are zero.

DCLK Bit Definition

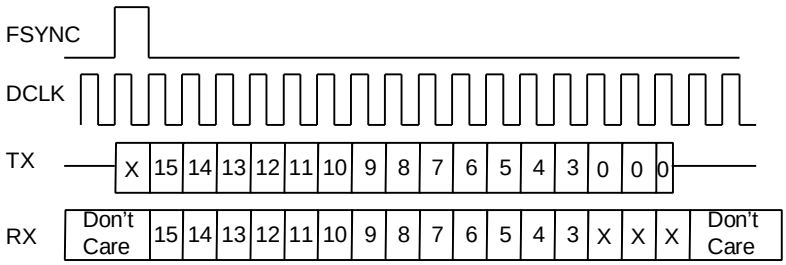
DCLK2	DCLK1	DCLK0	CLK_IN	Min Input	FSYNC	DCLK
0	0	0	13MHz	700mVp/p	8kHz(IN)	512kHz(IN)
0	0	1	13MHz	700mVp/p	8kHz(OUT)	200kHz(OUT)
0	1	0	16.8MHz	700mVp/p	8kHz(OUT)	200kHz(OUT)
0	1	1	19.44MHz	1Vp/p	8kHz(OUT)	360kHz(OUT)
1	0	0	19.44MHz	1Vp/p	8.1kHz(OUT)	202.5kHz(OUT)
1	0	1	8.4MHz	700mVp/p	8kHz(OUT)	200kHz(OUT)

The serial interface uses short frame sync. Data is transmitted and received in a two's compliment format. The FSYNC pin is held high for one falling DCLK edge. The PCM data word is output on the TX pin, beginning with the following rising edge of DCLK. Data is transmitted beginning with the MSB. Since the CODEC is 13 bits, the last three bits are zero. This results in the TX output going low impedance with the rising edge of FSYNC, and remaining low impedance until the middle of the MSB (16 and one half DCLK cycles). At power up the CODEC will release the TX line to be low impedance beginning with the third rising edge of FSYNC if DCLK[2:0] = 0. If any other DCLK mode is selected then GCAP II is the master of FSYNC and TX will be valid whenever an FSYNC occurs.



If FSYNC is high for one falling edge of DCLK, then GCAP II will start latching the 16 bit serial word into the receive data input on the following 16 falling edges of DCLK. GCAP will count the DCLK cycles and transfer the PCM data word to the D/A converter on the rising DCLK edge after the LSB has been latched.

The timing diagram below summarizes the serial interface operation.



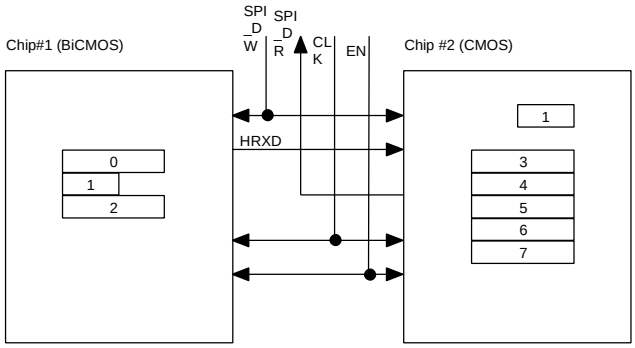
3.4 SPI Programming Interface

3.4.1 SPI Pin Description:

SPI_DW: serial data input line.
SPI_DR: serial data output line.
CLK: clock input line, data shifting occurs at the rising edge of this signal.
CE: clock enable line, active high.

Note that data is latched into GCAP II after the last valid bit of the addressed register has been loaded. GCAP II does NOT latch data on the falling edge of CE. For example, if address is 010 then after bit 13 is loaded the data will latch and the remaining bits of the field are ignored. If the address is 111 then after bit 25 is loaded the data will latch.

GCAP II is actually composed of two die. In one packaging option these two die are packaged separately. In this situation the two ICs can run SPI independently. If they are packaged together the interconnect is as shown below. SPI_DW, CLK, and EN are connected in parallel HRXD daisy chains to the CMOS IC before routing out as SPI_DR.

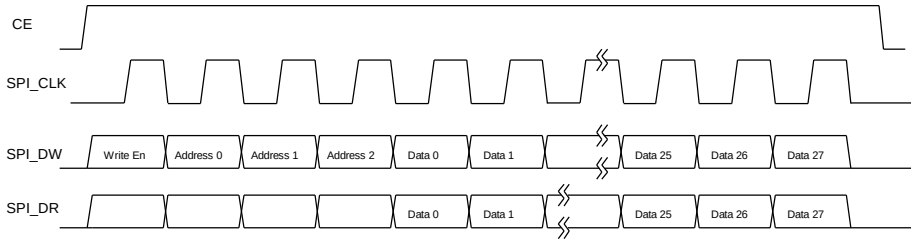


3.4.2. SPI Operation Requirements

1) The maximum clock rate is recommended at 5MHz.
2) All inputs have to be above 0.7*V2 for a logic 1 and below 0.3*V2 for a logic 0.
3) Data are transmitted least significant bit first. Data from the next SPI segment is transmitted from the output of the read data string if excess clocks are received.
4) Data and SPI_CLK signals will be ignored as long as CE has been low (logic 0) for at least 5nsec. SPI_DR will be tri-stated if CE is programmed low.
5) CE should be active (logic 1) only during the serial data transmission.
6) All write data is sampled at the rising edge of the SPI_CLK signal. Transitions on SPI_DW occur at least 5ns after the rising edge of SPI_CLK and stabilize before the next rising edge of SPI_CLK.
7) All read data is updated at the falling edge of the SPI_CLK signal. Transitions on SPI_DR occur at least 5ns after the falling edge of SPI_CLK and stabilize before the next falling edge of SPI_CLK.
8) CE has to be active (logic 1) at least 10nsec before the rising edge of the first SPI_CLK signal, and has to remain active (logic 1) at least 10nsec after the last rising edge of SPI_CLK. The recommended time interval for both cases is half a clock cycle. CE must remain inactive (logic 0) for at least 30nsec to latch in the data.
9) Coincident rising or falling edges of SPI_CLK and CE are not allowed. If the SPI_CLK signal is to be held at a logic 1 after the data transmission, the falling edge of the SPI_CLK signal must occur at least 5nsec. before CE becomes an active logic 1 for the next set of data.
10) If CE goes low before enough bits are sent then any write will be aborted.

3.4.3. SPI Operation Description:

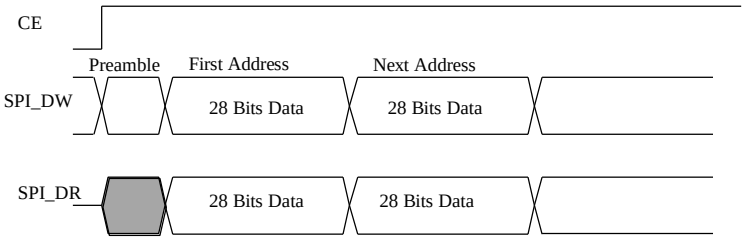
The control bits are organized into 8 fields. Each of these fields may contain up to 32 bits. A maximum of 28 bits are used per field with the remaining four bits used to address the 8 fields and to inhibit writing if only a read from GCAP II is desired.
For each SPI transfer, a one is written to the SPI_DW pin if this SPI transfer is to be a write. A zero is written to the SPI_DW pin if this is to be a read command only. If a zero is written, then any data sent after the address bits is ignored and the internal contents of the field addressed does not change when CE transitions from high to low. Next the three bit address is written to the SPI_DW pin LSB first. Finally, data bits are written to the SPI_DW pin LSB first. Once all the data bits are written then CE transitions from high to low to complete the SPI sequence.
Note that not all bits are truly writeable. For instance, it does not make sense to write an interrupt. Refer to the individual subcircuit descriptions to determine the read write capability of each bit.
To read a field of data, the SPI_DR pin will output the data field pointed to by the three address bits loaded at the beginning of the SPI sequence.
Below is a diagram showing the details of an SPI transfer.



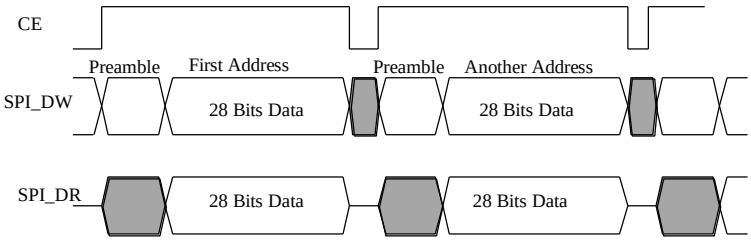
3.4.4 SPI Addressing Modes

Three addressing modes are supported.
Mode 1 is used in IC test. It allows continuous reading and writing of the SPI. Once the SPI address reaches 111 it rolls over to 000 and continues.
Mode 2 is for normal radio operation. It allows reading SPI addresses one at a time.
Mode 3 is a partial read mode. As many bits as desired can be read. If write is enabled then a write will occur once all valid bits of the addressed field have been loaded.

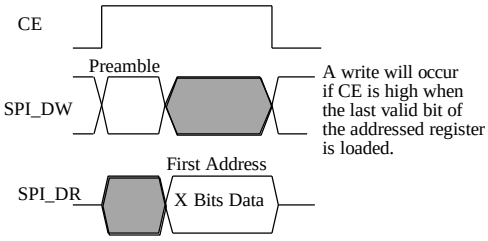
1) Contiguous Read/Write



2) Register Read/Write



3) Partial Read



3.4.5 SPI Data Structure:

	Address 000	**Address 001**	**Address 010**	**Address 011**	**Address 100**	**Address 101**	**Address 110**	**Address 111**
Bit	Bit Name	Bit Name	Bit Name	Bit Name	Bit Name	Bit Name	Bit Name	Bit Name
0	AUDOS1	LOST	UNUSED	TODA16	TOD16	ST4	DWNEN	ATO3
1	AUDOS0	LOSTC	MUTE1	TODA15	TOD15	ST3	DSCEN	ATO2
2	A2ON	TODAI	MUTE_EN	TODA14	TOD14	ST2	DF_RESET	ATO1
3	V1L	TODAM	EXT_CLK	TODA13	TOD13	ST1	AUDOHP	ATO0
4	VS1L	1HZI	AUX_LSEN	TODA12	TOD12	ST0	ADITH	ADEN
5	SQP	1HZM	MONITOR	TODA11	TOD11	DAY14	AUDOG2	ASC
6	V2L2	3SECI	CH_EN	TODA10	TOD10	DAY13	AUDOG1	DAC7
7	V2L1	3SECM	LIADC	TODA9	TOD9	DAY12	AUDOG0	DAC6
8	V2L0	ONOFFI	PA_ON2	TODA8	TOD8	DAY11	ALM	DAC5
9	V3L2	ONOFFM	PA_ON1	TODA7	TOD7	DAY10	AUDIHP	DAC4
10	V3L1	ONOFF2I	PA_B3	TODA6	TOD6	DAY9	AUDIS1	DAC3
11	V3L0	INT/EXTI	PA_B2	TODA5	TOD5	DAY8	AUDIS0	DAC2
12	ENVR	INT/EXTM	PA_B1	TODA4	TOD4	DAY7	AUDIG3	DAC1
13	ENV1	PWRONI	PA_B0	TODA3	TOD3	DAY6	AUDIG2	DAC0
14	STVR	PWRONM	TX_EN	TODA2	TOD2	DAY5	AUDIG1	ADD7
15	STV1	OVERI	AUX_EN	TODA1	TOD1	DAY4	AUDIG0	ADD6
16	SWMB2	OVERM	MAIN/AUX	TODA0	TOD0	DAY3	FS_INV	ADD5
17	SWMB1	MOBPORTI	CHECK			DAY2	CLK_INV	ADD4
18	SWMB0	MOBPORTM	IDH0			DAY1	CDBYP	ADD3
19	SWMA2	ONOFFSNS	IDH1			DAY0	DCLK2	ADD2
20	SWMA1	ONOFFSNS2	IDH2			IDJ0	DCLK1	ADD1
21	SWMA0	MOBSENSB	PCEN			IDJ1	DCLK0	ADD0
22	STSKA	PWRONSNS				IDJ2	CDC_TEST3	ADA3
23	STSKB	INTEXTSNS					CDC_TEST2	ADA2
24	ENSKA						CDC_TEST1	ADA1
25	ENSKB						CDC_TEST0	ADA0
26	A1CRTL						CDC_EN	

3.4.6 SPI Initial Conditions:

The following is a list of initial states for the data bits which need initial states.

GCAP II Pass 2.7

SQP	0	STSKA	0	STSKB	0	ENSKA	0
ENSKB	0	STV1	0	STVR	0	ENV1	1
ENVR	1	VS1L	1	V1L	0	V2L0	0
V2L1	0	V2L2	0	A2ON	0	DCLK0	0
DCLK1	0	DCLK2	0	CDBYP	0	CLK_INV	0
FS_INV	0	DF_RESET	0	AUDIS0	0	AUDIS1	0
ALM	0	AUDOS0	0	AUDOS1	0	ADITH	0
ASC	0	ADEN	0	DAC7	0	DAC6	0
DAC5	0	DAC4	0	DAC3	0	DAC2	0
DAC1	0	DAC0	0	EN	1	LOSTC	0
CH_EN	0	MONITOR	0	LIADC	0	PA_ON1	0
PA_ON2	0	MUTE_EN	0	MUTE1	0	MUTE2	0
DSCEN	1	DWNEN	1	EXT_CLK	0	3SECM	0
1HZM	0	TODAM	0	PWRONM	0	INTEXTM	0
OVERM	0	ONOFFM	0	MOBPORTM	0	TX_EN	0
AUX_EN	1	CDC_TEST3	0	CDC_TEST2	0	CDC_TEST1	0
CDC_TEST0	0	CDC_EN	0	A1CRTL	0	CHECK	0

GCAPII Pass 3.0 initial state changes

AUX_LSEN	0	PA_ON2	1	PA_B3	1	PA_B2	1
PA_B1	0	PA_B0	0	PCEN	0	AUDOHP	0
AUDIHP	0	EN	deleted				

Note: The above table lists the additions to the GCAPII pass 2.7 initial state table. Also the EN bit no longer exists

3.4.7 SPI programming requirements

Address 000 Initial State

Bit#	Label	Initial state pass 3.0
0	AUDOS1	0
1	AUDOS0	0
2	A2 ON	0
3	V1L	0
4	VS1L	0
5	SQP	0
6	V2L2	0
7	V2L1	0
8	V2L0	0
9	V3L2	0
10	V3L1	0
11	V3L0	0
12	ENVR	1
13	ENV1	1
14	STVR	1
15	STV1	0
16	SWMB2	1
17	SWMB1	0
18	SWMB0	0
19	SWMA2	1
20	SWMA1	1
21	SWMA0	0
22	STSKA	0
23	STSKB	0
24	ENSKA	0
25	ENSKB	0
26	A1 CRTL	0
27	0	0

The initial state of address 000 is dependent on the configuration of three hardware pins (PGM2, PGM1, and PGM0) see section 3.1.1 for state definitions. The above table defines the initial states for Kramer as of 8/10/98. These pins predetermine the states for switching supplies PWM1, PWM2 and LDO supply V3. Care must be taken when writing to these bits if the new state causes a hardware conflict the part may power down or damage itself. Bits 16-18 control PWM2 and Bits 19-21 control PWM1. The PWMs are supplies for the linear regulators therefore the PWM must not be programmed lower than the voltage the linear regulator is programmed to regulate to. Likewise the linear regulators which are controlled by bits 3,4,6-15 must not be

programmed to regulate a voltage higher than that which it is supplied with. The linear regulator must be powered down before or simultaneously with the PWM feeding it.

Address 000 register after SW Init.

Bit#	Label	SW Init. state pass 3.0 with V3 @ 2.0V
0	AUDOS1	0
1	AUDOS0	0
2	A2 ON	0
3	V1L	1
4	VS1L	1
5	SQP	0
6	V2L2	0
7	V2L1	0
8	V2L0	0
9	V3L2	0
10	V3L1	0
11	V3L0	0
12	ENVR	1
13	ENV1	1
14	STVR	1
15	STV1	0
16	SWMB2	1
17	SWMB1	1
18	SWMB0	1
19	SWMA2	1
20	SWMA1	1
21	SWMA0	0
22	STSKA	0
23	STSKB	0
24	ENSKA	0
25	ENSKB	0
26	A1 CRTL	0
27	0	0

The above table lists the state that address 000 should be programmed to after reset for GCAP II. Kramer currently only uses the boost PWM supply therefore the buck PWM should be turned off. This should be performed as soon as possible. Care should be taken not to turn the buck PWM back on during a subsequent write. Note that the CHECK bit in address 010 must be set to 1 to change the switcher and regulator settings.

Address 010 Register after SW Init.

Bit#	Label	SW Init. state pass 3.0 with V3 @ 2.0V
0	UNUSED	0
1	MUTE1	0
2	MUTE_EN	0
3	EXT_CLK	1
4	AUX_LSEN	1
5	MONITOR	0
6	CH_EN	0
7	LIADC	1
8	PA_ON2	1
9	PA_ON1	0
10	PA_B3	0
11	PA_B2	0
12	PA_B1	0
13	PA_B0	1
14	TX_EN	0
15	AUX_EN	1
16	MAIN/AUX	0
17	CHECK	1
18	IDH0	X
19	IDH1	X
20	IDH2	X
21	PCEN	1
22		
23		
24		
25		
26		
27		

3.5 A/D and D/A

Read and write operations will be accomplished through the SPI bus.

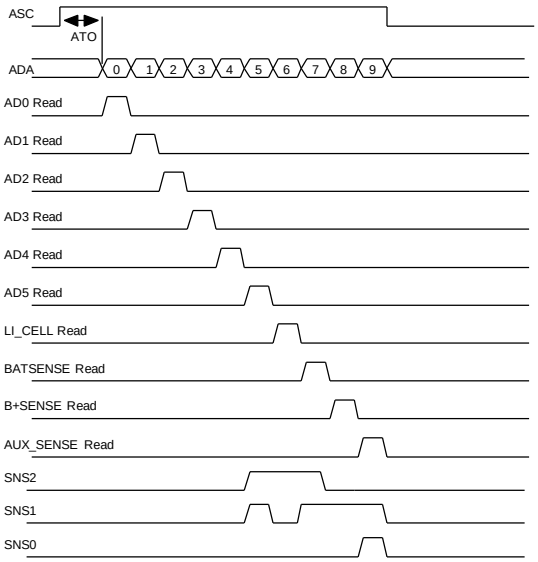
The DAC can be set by writing to DAC[7:0]. All zeros is the low power state. The DAC output is internally fed to the battery charger circuit and is not directly available at any output pin. The charger within GCAP II is not used in Kramer. (See 3.6 Battery Charger Operation)

The ADC is 8 bits with 10 inputs. CLK_IN must be present when using the A/D converter. Input address 7 (ADA[3:0] = 0111) is internally connected to the output of BATSENSE. Input address 8 (ADA[3:0] = 1000) is internally connected to the output of B+SENSE. Input address 9 (ADA[3:0] = 1001) is internally connected to the output of AUX_SENSE. Input address 6 (ADA[3:0] = 0110) has a high input impedance buffer and is internally connected to LI_CELL. These inputs are not directly accessible at any output pin. The other 6 A/D inputs are available as AD0 through AD5.

The ADC will have the ability to execute a conversion in two ways:
1) Enable the conversion with the Start Convert (ASC) bit.
2) Enable the conversion with the rising edge of the ADTRIG signal.

In both of the above cases the conversion will begin after a delay set by the ATO register. This register will be 4 bits long and will be driven by CLK_IN/256.

Once conversion is initiated all 10 channels will be sequentially converted and stored in registers. This is shown in the diagram below. The signals labels SC0-2 refer to the interdie connections to control the SNS_OUT addressing.



To convert multiple channels starting the conversion with the SC bit, the following steps are executed:

1) Enable A/D. (ADEN=1)
2) Start conversion at channel 0 by writing a 1 to the start conversion bit. (ASC) The conversion will begin once ATO counts down to zero.
3) Wait for completion. (ASC will reset to zero when complete.)
4) Write the result address. (ADA[3:0]) Note that it is possible to write the starting address of the next SPI read while reading out the present data.
5) Read conversion values.
6) Repeat steps 5 and 6 for all channel results.

To convert multiple channels starting the conversion with the rising edge of ADTRIG, the following steps are executed:

1) Enable A/D. (ADEN=1)
2) The conversion will automatically start at channel 0 once ATO counts down to zero.
3) Wait for completion. (ASC will reset to zero when complete.)
4) Write the result address. (ADA[3:0]) Note that it is possible to write the starting address of the next SPI read while reading out the present data.
5) Read conversion values.
6) Repeat steps 5 and 6 for all channel results.

A/D and D/A Bits Definition (all are R/W)

Name	# of Bits	Description
ASC	1	Logic high starts A/D conversion. This bit will self clear when the conversion is complete.
ADEN	1	Logic high enables the A/D converter.
ADA[3:0]	4	Selects the results register read when reading the A/D data.
ADD[7:0]	8	The value of the last conversion for the channel selected by ADA[3:0]. Read only.
DAC[7:0]	8	Data used for the D/A conversion. A read of this register is used for testing purposes.
ATO[3:0]	4	Delay from the A/D trigger event until conversion begins.

3.6 ~~3.6~~ Battery Charger Operation

The GCAP II IC contains an on-board rapid charger, whose charge capability is controlled by an on board D/A. The GCAP II monitors battery voltage and the call processor monitors battery type in order to determine the manner in which to charge the battery. The GCAP II contains an error amplifier and a feedback amplifier. An external pass device (FET) and sense resistor account for the remainder of the charge circuit. External connections for the charger on the GCAP include ISENSE, CHRGC.

3.6.1 ISENSE

ISENSE is an input for measuring the voltage across the external sense resistor (0.24 ohm). The voltage difference measured is fed to the feedback amp in GCAP II.

3.6.2 CHRGC

CHRGC is an output from the internal error amplifier that drives the gate of the external FET accordingly. The FET passes current from EXT_B+ to the battery to be charged.

The following table shows the relationships between the D/A counts and charger capability.

D/A Code	I BATT	Comment
0	0	OFF

10		Still may be OFF
21		ON
128	480mA ±50mA	
255	1.000A±100mA	Full Scale

3. 7 A/D Thresholds

3.7.1 B+

Lithium ion thresholds

Description	Voltage	A/D	HEX
Standby: Software Shutdown	2.85	49	31
Standby: Battery Bar 1 Off	3.5	85	55
Standby: Battery Bar 2 Off	3.65	94	5E
Standby: Battery Bar 3 Off	3.8	102	66
Transmit: Software Shutdown	2.85	60	3C
Transmit: Battery Bar 1 Off	3.05	68	44
Transmit: Battery Bar 2 Off	3.2	80	50
Transmit: Battery Bar 3 Off	3.4	28	1C
Vb+sense=((B+)-1.98)*0.55			

3.7.2 BATT+

Description	Voltage	Scaled Voltage	A/D	HEX
Battery Minimum	TBD	TBD	TBD	TBD
Battery Maximum	TBD	TBD	TBD	TBD
Vbattsense=((BATT)-1.33)*0.60				

3.7.3 Thermistor (AD2)

Temp(C)	Rth(Dale)	V(NTC)	DAC value	HEX
NO BAT	infinity	2.75	255	FF
-40	336.6	2.695	255	FF
-35	242.8	2.665	255	FF
-30	177	2.627	255	FF
-25	130.4	2.577	255	FF
-20	97.12	2.516	255	FF
-15	72.98	2.441	249	F9
-10	55.34	2.35	240	F0
-5	42.34	2.245	229	E5
0	32.66	2.125	217	D9
5	25.4	1.991	203	CB
10	19.9	1.847	188	BC
15	15.71	1.696	173	AD
20	12.49	1.541	157	9D

25	10	1.388	142	8E
30	8.06	1.238	126	7E
35	6.53	1.096	112	70
38	5.88	1.0229	104	68
40	5.33	0.964	98	62
45	4.37	0.844	86	56
50	3.6	0.735	75	4B
55	2.99	0.639	65	41
60	2.49	0.553	56	38
65	2.08	0.478	49	31
70	1.75	0.413	42	2A
75	1.48	0.358	36	24
80	1.26	0.31	32	20

3.7.4 DOWNLINK (AD4)

DSC Downlink

	Typical	Max	Min
V1	5	5.15	4.85
R1 +/- 5%	22000	24420	19580
R2 +/- 5%	100000	105000	95000
R3 +/- 5%	100000	105000	95000

Accessory Type	Typical	Pull Down resistor R4 Max +5%	Min - 5%	Typical	A/D voltage Max	Min	Typical	DAC value Max	Min	DAC ranges
NONE	none	None	none	2.252	2.463	2.053	230	251	209	201
DHFA	56000	58800	53200	1.663	1.896	1.451	170	193	148	145
Data	22000	23100	20900	1.185	1.393	1.003	121	142	102	<145

3.7.5 DSC_EN (AD3)

DSC_EN Definitions

	Typical	Max	Min
V1	5	5.15	4.85
R1 +/- 5%	10000	10500	9500
R2 +/- 5%	100000	105000	95000
R3 +/- 5%	100000	105000	95000
R5 +/- 5%	147000	154350	139650

Accessory		Pull Down resistor R4			A/D voltage			DAC value		DAC
Type	Typical	Max +5%	Min -5%	Typical	Max	Min	Typical	Max	Min	ranges
IGN Low	none	None	none	2.24	2.44	2.04	228	249	208	194
IGN Hi	22000	23100	20900	1.59	1.77	1.40	162	180	143	138
Data	22000	23100	20900	1.59	1.77	1.40	162	180	143	138

3.7.6 MAN_TEST (AD5)

MAN_TEST Definitions										
	Typical	Max	Min							
V1	2.775	2.85	2.7							
R1 +/- 5%	10000	10500	9500							
Accessory		Pull Down resistor R4			A/D voltage			DAC value		DAC
Type	Typical	Max +5%	Min - 5%	Typical	Max	Min	Typical	Max	Min	ranges
NONE	none	none	none	2.775	2.85	2.7	255	255	255	250
FAST CHRG	33000	34650	31350	2.130	2.237	2.023	217	228	206	180
Off hk										
MID CHRG	10000	10500	9500	1.388	1.496	1.283	142	153	131	102
off hk										
	33K || 3.3K									below
FAST CHRG	3000	3150	2850	0.640	0.710	0.576	65	72	59	102
On hk										

Note: Software uses MAN_TEST in a test mode if MAN_TEST is grounded.

3.8 RTC Module

The RTC module is contained in GCAP2. Its power source is hardware-switched between an internal supply and an external rechargeable (secondary) battery. The charge circuit for the battery is internal to GCAP and is switched on and off via SW control. The module counter uses an external 32.768khz xtal.

The RTC in the first phase of Kramer will be similar to the StarTac implementation, in that only hours and minutes will be displayed. The format will be user selectable in 12-hour or 24-hour mode.

The time will be displayed in the graphics area of the LCD. In StarTac it was displayed as a separate icon. The time will be displayed after the wake-up message has terminated and until the user presses a key or goes into the menu. Once the user has cleared the display (ended a call, exited menus, clearing key presses) the time will reappear in the display. The graphical size of the digits is *in the marketing requirements document*.

The voltage of the rechargeable battery will be read using the Li_Sense A/D in GCAP. The formula for the Li_Sense is (Li_Cell-0.93)*0.70, where Li_Cell is the battery voltage.

When Li_Cell discharges to a voltage of 2.3V the charger should be switched on and remain on until Li_Cell reaches a voltage of 2.8V, at which point it is switched off.

Li_Cell Voltage	DAC Value
2.8V	133
2.3V	100

The rechargeable battery can and will be charged off of any power source (main battery, CLA, etc).

There is no phasing requirement for the secondary cell.

4 WHITECAP LOGIC INTERFACES

4.1 DSC Module

The DSC module implements the GSM Data Speech Control interface in the Whitecap IC. It accepts manchester encoded data input on the DSC bus and generated manchester coded data onto the DSC bus. DSC data may be transmitted to or received from the TI LEAD megamodule or TI ARM megamodule via the XIO interface and PIF interface, respectively. The PIF interface also provides control of the DSC module.

The DSC module generates a clock and frame sync to the audio codec interface. The frame sync is synchronized so the DSC LEAD interrupt occurs at the same time as the Audio CODEC interrupt. An ARM interrupt is generated to synchronize the ARM megamodule to the DSC interrupt.

The DSC time slots are the basic data structures in the DSC module. The function of the DSC is to transmit and receive DSC frames on the DSC bus. These frames may come from or be sent to the Lead DSP Audio Coder XIO port, the ARM Call Processor PIF port, or the Manchester coded DSC bus.

The DSC module in Whitecap operates only in the Master mode at a controllable bit rate of 128kHz or 512kHz. The audio CODEC clock always operates at 512Khz. Switching the DSC from 128kHz to 512kHz is held off until DSC time slot boundaries. This functionality is changed from BIC 4.X for the Whitecap DSC module to accommodate the CODEC interface and synchronization for the Lead DSP.

4.2 UART - RS232

The UART is based upon a TL16C550 compatible UART. It is used to communicate serially over an RS232 interface. Refer to TI document BRK_UART ver: 1.1 for detailed information.

The module sends and receives characters of 8bits. The number of stop bits can be programmed to 1 or 2. Parity can be programmed to even, odd, or disabled completely. The module contains a 32 deep FIFO for the received characters and a 16 deep FIFO for transmit. It generates its own baud rate based upon a programmable divisor and its input clock.

4.2.1 BATTERY SERIAL DATA COMMUNICATION (development board only)

~~Kramer will not support this feature.~~

The feature is used to communicate via the UART interface with the serial ROM inside the "Smart" battery (Lithium-Ion).

This port is also used to read data contained in a serial ROM device like the Dallas DS2401 integral part of the security scheme implemented in other DCS phones design.

4.3 SIM INTERFACE

The SIM Interface is a peripheral in the Whitecap Chip that allows the ARM Core to communicate with pre-paid cards or SIM cards. It communicates with the ARM via the 16-bit internal Peripheral Bus. The SIM interface contains 2 ports, one allowing synchronous or asynchronous (pre-paid cards) serial transmission and the other allowing only asynchronous serial transmission.

4.3.1 GCAPII / SIM CARD INTERFACE

Kramer can support both 3V and 5V SIM Cards. GCAP II contains level shifters that can translate 5V logic down to 3V. If a 3V SIM card is present it will merely be buffered through to Whitecap.

SIM Card Block	GCAP II Level Shifter Input	GCAP II Level Shifter Output	Comments
RESET - Input to SIM Card	LS2_INTG1A, ball K7	LS2_OUT_TG1, ball J7	
CLOCK - Input to SIM Card	LS1_IN, ball G6	LS1_OUT, ball F6	3.25 Mhz provided by WCP
SIMPD - Output to WCP			
SIM I/O – Input/Output	SIMI_O, ball J8	LS3_TX and LS3_RX, balls K10 and H8	
VCC			VSIM1, 5.0V
VPP			VSIM1, 5.0V

Table X. GCAPII - SIM CARD INTERFACE

The phone will always assume that it is talking to a 5 volt SIM card since 3 volt SIM cards are required to operate at 5 volts. This way on power up, VSIM is programmed to 5 volts. RESET and CLOCK will come from Whitecap at 3 volts and be level translated to 5 volts in GCAP II before being sent to the card. SIM I_O is a serial data communication line that is connected in a wired-or configuration.

4.3.2 GCAPII / WHITECAP INTERFACE

The Whitecap chip SIM Peripheral contains a UART and a Synchronous Transceiver. Control bits are set through the ARM interface and control the overall function of the SIM interface for both the UART and the Synchronous Transceiver. The control registers control operation of mode, baud rate, enables, status, interrupt conditions, and interrupt masks. SIM auto power down and presence detect are also handled by writing and reading SIM registers.

Kramer will operate using a SIM in asynchronous mode (Port 1). This will be the default normal operation for the phone.

4.3.3 SIM CLOCK

The SIM peripheral receives a 13 Mhz clock. Within the module, this clock is divided down in frequency for the respective transceivers. For the synchronous SIM, clocks are generated to provide a 13 Mhz "divide_by_32" and 3.25 Mhz "divide_by_8" clock. The clock derivatives are controlled by the Control Register Setting (CSRC). Within the synchronous transceiver, both of these clocks are further divided down

by 40 before being sent to the SIM card. This clock is approximately 13 kHz. Internally, the SIM also requires a 13 Mhz "divide_by_2" and a 3.25 Mhz "divide_by_2".

For the asynchronous SIM, the clock generated and sent to the SIM card is basically a 13 Mhz or 3.25 Mhz clock (Again, chosen according to the setting of Control Register CSRC). For port 1, which only allows asynchronous operation, the clock to the card is this system clock. For port 2, the clock may be either Synchronous or Asynchronous depending on the type of SIM card connected to the port (Determined by control register settings). Internally, the asynchronous SIM receive and transmit functions will use clocks that are selected by the baud rate.

4.3.4 Synchronous Transceiver (Kramer will not support this feature)

The synchronous transceiver's function is to communicate with a pre-paid card. The pre-paid card requires different modes of operation. These modes are defined sequences that the interface must follow. The modes include reset, read, and special writes. Control bits are used to control the state machine that implements the required transitions for these modes. Refer to SIM Interface Specification pp. 6 - 15 for more detailed information regarding the Synchronous Transceiver.

4.3.5 UART

The SIM UART consists of a receiver, transmitter, special logic to detect auto power down of ports, and sim card presence detection. It facilitates transmitting and receiving data with a SIM card. The asynchronous SIM card interface does not have the same type of modes that the Synchronous transceiver has. In the UART, the "mode" is a baud rate that can be selected for the receive and transmit.

The SIM UART baud rate selector provides different sampling rates for the transmitter and receiver. Based on the selected baud rate, the receiver will serially receive data from the SIM card and collect the data in a pre-defined fifo queue. Also, for the selected baud rate the transmitter accepts data loaded into a shift register and serially transmits data to the SIM card. The receive and transmit functions include parity checking, interrupt generation, and interrupt enables. The data to be transmitted or received is expected to include a start bit, 8 data bits, parity bit, and 2 stop bits.

Besides the receive and transmit functions, the SIM auto power down logic allows the ability to power down a port. The SIM cards reset, clock enables, transmit enables, and VCC enables are controlled when the SIM auto power down (SAPD) is detected.

This implementation of the SIM UART includes the overall muxing of busses for the Synchronous SIM and is where all of the control registers reside for the entire SIM card interface module. Refer to SIM Interface Specification pp. 16 - 23 for additional information on the UART as well as descriptions for the control bits and programming information.

4.4 Keypad Interface

The keypad interface consist of 5 rows and 5 columns pins. The rows are Inputs and the columns can be configured as Inputs or Outputs by setting bit 5 of the COL_CONTROL register (1=Input, 0=Output).
When operating with columns as inputs, any active row or column signal will result in an interrupt.
The active state (High or Low) for columns and rows can be selected by setting bit 2 of the COL_CONTROL and ROW_CONTROL respectively.

4.4.1 3 Element Keypad

NOTE: *The 3 elements keypad approach it is not supported by WCP RAM1A parts. For these parts Kramer will use the 2 element keypad standard approach.*

The keys on the PCB use a three contact design instead of the two of previous configurations. One of the contacts is tied to ground while the other two are pulled high (2.7 V) and connected to the rows and columns inputs. When a key is pressed all three of its pads are shorted and therefore grounded. Each key is uniquely distinguished by the two lines pulled low. No strobing of the keypad is necessary.

The table below shows the current keypad mapping.

Function	Keys	KBC4	KBC3	KBC2	KBC1	KBC0	KBR3	KBR2	KBR1	KBR0
1	1							0	0	
2	2							0		0
3	3		0					0		
4	4			0				0		
5	5				0			0		
6	6					0		0		
7	7								0	0
8	8		0						0	
9	9			0					0	
*	10				0				0	
0	11					0			0	
#	12		0							0
OK	13			0						0
VA	14				0					0
FAST ACCESS	15					0				0
M+	16		0	0						
CLEAR	17		0		0					
MENU	18		0			0				
MAIL	19			0	0					
VOL_UP	20			0		0				
VOL_DWN	21				0	0				
SMART	22						0			0
HOOKSW										

As indicated above, hookswitch is not in the keypad matrix. Hookswitch is detected on IRQ0. A falling edge on this line will indicate hookswitch being closed. It will remain low until hookswitch is opened again.

4.5 Memory Interfaces

The WCP chip has access, via its parallel data bus, to one SRAM (64k X 16) in a 48 ball uBGA, one 16Mbitx16 Read-While-Write capable Flash EPROM in a 48 ball uBGA (this part combines EEPROM and Flash ROM functionality), and graphical display.
Each of these devices are assigned specific chip selects from the WCP.
Within the WCP chip select control register, the wait states are defined for each device. Each wait state is the equivalent of one clock cycle, i.e. 1/13 MHz = 77 ns.

4.5.1 Flash

4.5.1.1 Read While Write (RWW) Capability

The part described in this document is a 8Mbitx16, Read-While-Write (RWW) capable Flash EPROM in a 48 ball uBGA package. RWW capability is achieved through the BGO (Back Ground Operation) mode of operation. The BGO feature of the device allows Program or Erase operations to be performed in the background on BGO blocks while the device simultaneously allows Read operations to be performed on the main memory blocks.
The memory partition is shown in section XX. The upper partition consists of equally sized data blocks of either 16kwords or 32 kwords. The lower partition consists of at least three BGO blocks and a boot block. The boot block is 8 kwords in size. The BGO blocks will total from 12 kwords to 24 kwords in size.

Functionality/Definitions of the part include:

Partition -- Indicates the division between the group of data blocks and the BGO blocks.
Upper Partition -- Address space consisting of data blocks.
Lower Partition -- Address space consisitng of BGO blocks and boot block.
Erase-Suspend -- Able to read or write to any BGO block while erase-supended in another BGO block.
Write-Suspend -- Able to read from any BGO block while write-suspended in another BGO block.
Read-While-Write -- Able to read from any data block while simultaneously writing to or erasing from any BGO block.

The part will operate at a read voltage of 2.7V minimum and a write voltage of either 2.7V or 5V. The access time of the part is 120 ns over the industrial temperature range of -40 to +85 C.
The Flash shall be partitioned as shown in Figure 1:

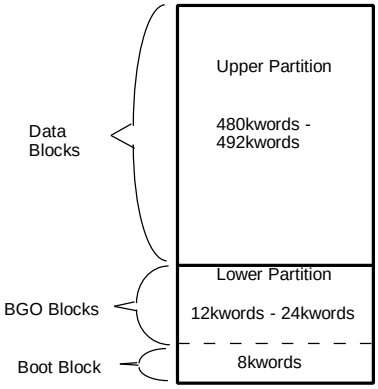


Figure 1: Memory block segments

The lower partition consists of several BGO blocks and a boot block totaling 48kwords maximum. The boot block begins at the lowest address and is 8kwords in depth. There should be at least three BGO blocks in the lower portion with a maximum size of 16kwords each but the sum not exceeding 24kwords.
The Upper Partition consists of either 16kword or 32kword data blocks totaling 480kwords - 492kwords.

Programming Requirements

Byte/Word location programming is required for this device. Also, every bit location within a word, must be capable of withstanding a minimum of sixteen repetitive writes to any bit within the word without damage to

the cell. Further, the device must be capable of withstanding the 16 repetitive writes in consecutive byte/word locations. Write latency requirements are expected to be maintained with the repetitive write requirement.

Latency and erase cycle

Latency is defined to be the duration of any write cycle or erase suspend cycle within the boot, parameter, or data blocks at a minimum. Erase suspend provides access to the array before the completion of an erase cycle. Upon re-entering the erase cycle, the part should continue from where it was suspended. The entire erase cycle for a block is the cumulative total the erase cycle is active. The state machine should not reset during the suspend command.

4.5.2 EEPROM

The feature of the part described above shall serve the purpose of EEPROM replacement.

4.5.3 SRAM

Kramer will use the standard 64Kx16 part currently used in the DCS Modulus.

4.5.4 Chip Select Assignments

The WCP chip supports 10 programmable chip selects with programmable start address, block size and bus width (8 or 16 bits).
The table below shows the current chip select assignment

Pin Name	Ball #	Type	Active H/L	Description
CE0	D9	O	L	Flash ROM CS
CE1	A9	O	L	Flash ROM OE
CE2	C9	O	L	RAM Byte Control 1
CE3	E9	O	L	RAM Byte Control 1
CE4	A10	O	L	Unused
CE5	D10	O	L	Unused
PA3/CE6	E10	I/O	L	DP_EN (LCD CS)
PA2/CE7	A11	I/O	L	Configured as A21 for 32M FLASH support
PA1/CE8	B11	I/O	L	Optional can be config. as GPIO on port A
PA0/CE9	C11	I/O	L	VRVA_OUT

4.5.5 Byte Accessing Memory Interface

4.6 GPIO PORT ASSIGNMENT

The General Purpose I/O control and status controls a total of thirty-two (32) bi-directional I/O pins. Each I/O pin can be programmed via the peripheral bus interface. Refer to the BRK_GPIO version 1.3 document by Kevin Parmenter for specifics of the configuration of the WCP I/O pins. Below is a table of all GPIO signals and their uses.

Table.

GPIO	Pull UP/DN ROM part only	Altern. Fun.	I/O	Active H/L	Signal	Description
PA0	PU	CE9	O		VRVA_OUT	VR/VA Int Out
PA1	PU	CE8				DSP Reserved
PA2	PU	CE7				SW Reserved temp.
PA3	PU	CE6	O	L		Display Enable
PA4	PU	UART UCTS				Open
PA5	PU	UART URTS	O	L	RCTS/EXT_CHG_EN	
PA6	PU	MAN_DCD	O	H	CLK_SELECT	PLL,26MHz/2
PA7	PU	Timing 8				*DSP Reserved
PA8	PU	Timing 7				*DSP Reserved
PA9	PU	Timing 6	O	H	ADTRIG	GCAP A/D Trigger
PA10	PU	Timing 5	O	H	TX_EN	
PA11	PU	MQSPI_CS2				DSP Reserved
PA12	PU	MQSPI_CS3				DSP Reserved
PA13	PU	IRQ4	I		VRVA_IN	
PA14	PU	IRQ3	I	L	DCABLE_INT	Data Cable Interrupt
PA15	PU	IRQ2	I	L	HEAD_INT	Boom Headset Interrupt
PB0	PD (RAM part has PU)	PWM_0	O	H	LED_GREEN	Green stat. LED Control
PB1	PD (RAM part has PU)	PWM_1	O	H	LED_RED	Red stat. LED Control
PB2	PD (RAM part has PU)	SVEN1_OUT				Reserved
PB3	PD (RAM part has PU)	CLK1_OUT				Reserved
PB4	PD (RAM part has PU)	RST1_OUT				Reserved
PB5	PD (RAM part has PU)	DATA1_TX_OUT				Reserved
PB6	PD (RAM part has PU)	INT_0	O	H	CHRG_EN	Internal Charge Enable
PB7	PD (RAM part has PU)	INT_1	O	H	DSC_EN	DSC Enable
PB8	PD (RAM part has PU)	INT_2	O	H	VIB_EN	Vibrator Control
PB9	PD (RAM part has PU)	INT_3	O	H	BKLT_EN	Backlight control
PB10	PD (RAM part has PU)	SIMPD_1	I	L		Reserved
PB11	PD (RAM part has PU)	DATA1_RX				Reseved
PB12	PD (RAM part has PU)					Reseved
PB13	PD (RAM part has PU)					
PB14	PD (RAM part has PU)		O	H	-5V_EN	-5V Control
PB15	PD (RAM part has PU)		O	L	BOOM_EN	HS_MIC Control

4.6.1 VR/VA (PA0,PA13)

4.6.2 RTS/EXT_CHG_EN (PA5)

With the data cable connected this output acts as the RTS output of the RS-232 UART. A ~~low~~ high on this pin indicates the RX FIFO of the UART is not full. A low~~high~~ indicates it is full and halts the PC's data transmission until software can process the pending bytes.
With the external charger present, this signal acts as EXT_CHG_EN. A low enables communication with the external charger. This signal should default high (inactive).

4.6.3 CLK_SELECT (PA6)

A high selects the PLL on magic for clock generation. A low selects 26MHz/2.

4.6.4 ADTRIG

4.6.5 TX_EN (TIMING 5)

See section 5.4.

4.6.6 DCABLE_INT (IRQ3)

See section 6.3.2 for the description of this signal.

4.6.7 HEAD_INT (IRQ2)

See section 6.3.1.

4.6.8 BI_COLOR LED Control (PB0, PB1)

Kramer uses a bi-color LED as in StarTac. When the flip is closed (hookswitch activated) ~~WhiteCap must control~~ the LEDs must flash every two seconds for a period of 100ms (100 ms ON, 1.9s OFF). Hardware shall control the flash period and duty cycle while displaying camp status.
PB0 controls the green LED and will go "high" when the radio is camped to its home system. PB1 controls the red LED and goes "high" when the radio is not camped. Both PB0 and PB1 will go "high" when the phone is roaming, creating an orange color. Software need only change the LED control line state for a change in camp status.
On an incoming call (flip closed) the green and red will alternate at ½ second intervals, continuously. During incoming call notification WhiteCap must control the LEDs directly. The -5V_EN signal shall switch control of the LEDs from hardware to software. During a location update the LED control lines should be inactive (driven low).
When the hookswitch is open PB0 and PB1 will be held "low" and there is no LED function. This timing is subject to change based on market requirements and radio performance.

Note: Hardware control of the LEDs is a planned feature. Currently the software must control the LED lines at all times.

4.6.9 CHRG_EN (PB6)

Active high enable for BATT_FDBK.

4.6.10 DCS_EN (PB7)

This active high output is level shifted to V1 for DSC_EN to the buttplug.

4.6.11 VIB_EN (PB8)

Active high to enable vibrator drive. This signal should only be driven when external power is not preset.

4.6.12 BKLT_EN (PB9)

Active high enable for backlight LEDs.

4.6.13 -5V_EN (PB14)

Active high enable for the –5V inverter. This signal should be active at least 2 frames before any TX. During a call this signal can be left active for the duration of the call.

4.6.14 BOOM_EN (PB15)

Should be set low when the boom headset is present and it is the active audio path.

4.7 WCP External Interrupt Sources

The mapping of the external WCP interrupts is as follows:

IRQ	Source	Description
0	HS_INT	Hookswitch Interrupt
1	GCAP_INT	GCAPII Interrupt
2	HEAD_INT	External headset interrupt
3	DCABLE_INT	Data cable interrupt
4	VRVA_IN	VRVA Interrupt from LEAD

4.8 DSP DEBUG SIGNALS

4.9 JTAG INTERFACE

JTAG refers to TI scan-based emulation which is based on the IEEE 1149.1 standard. A cable pod marked *JTAG 3/5V* interfaces with the XDS510 emulator and supports both standard 3 volt and 5 volt target system power inputs. The JTAG target devices support emulation through a dedicated emulation port. To communicate with the emulator, your target system (development board) must have a 14 pin header with the pinout shown below.

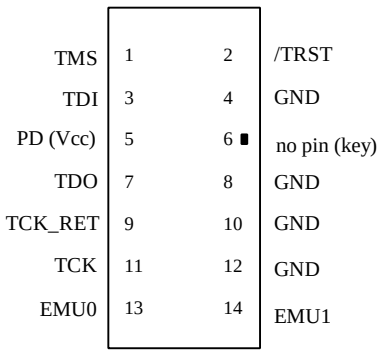


Figure X. JTAG 14 pin header pinout.

The following table provides a description of the signals used:

Table X. JTAG signal description

Signal	Description	Emulator State	Target State
TMS	Test Mode Select	O	I
TDI	Test Data Input	O	I
TDO	Test Data Output	I	O
TCK	Test Clock. TCK is a 10.368 Mhz clock source from the emulation cable pod. This signal can be used to drive the system test clock.	O	I
/TRST	Test Reset	O	I
EMU0	Emulation pin 0	I	I/O
EMU1	Emulation pin 1	I	I/O
PD (Vcc)	Presence detect. Indicates that the emulation cable is connected and that the target is powered up. PD is tied to V2 of GCAPII in the target system	I	O
TCK_RET	Test Clock Return. Test clock input to the emulator. May be buffered or unbuffered version of TCK.	I	O
GND	Ground		

Please refer to ARM MEGAMODULE EMULATION SPECIFICATION (Rev 1.1) by Iano D'Arrigo for additional information regarding WhiteCap emulation via JTAG.

4.10 ONE WIRE BUS

This feature will not be used in Kramer

4.11 DISPLAY INTERFACE

Kramer will support a 96x54 pixel dot matrix with additional indicators and icons.
The display is driven by the EPSON SED1568 controller. Temperature compensation and the negative voltage will be supplied by the SED1568.

Indicators and icons for the display will have a mapping compatible with previous similar display version (see StarTac and Modulus design). One new icon (Bell) will be added. This icon shall serve the purpose of Vibrator/Ring mode indicator. The bell will be displayed when the Ring feature is ON and will not be displayed when the vibrator is ON.

4.11.1 Contrast Control

The Kramer contrast shall be controllable via software. Display contrast is determined by a flexible default value and a user defined offset of +/- 5 steps. Each step shall correspond to two (2) DAC counts of the contrast control register of the 1568. The default value should be set at thirty-two (32).

4.11.2 Display Power Down Sequnce

The display should be powered down with the following sequence:

1. Write display off command.
2. Write all pixels on command.
3. Now the radio may be powered off

4.12 Deep Sleep Mode

The DSM (Deep Sleep Module) contained in the WCP chip will control the Deep sleep mode and wakeup functions. Deep sleep refers to the process by which the Layer 1 timer is disabled at a know 32KHz clock edge, all 13MHz peripheral are shut down, the system clock is gearshifted from 13MHz to 32KHz and the 13 MHz clock is turned off. Wakeup refers to the process by which the 13 MHz clock is turned on, the system clock is gearshifted from 32KHz to 13MHz, the 13MHz peripheral are started up, and the layer 1 timer is enabled at a known 32KHz clock edge.
WCP controls the STBY input to GCAP. Assertion of STBY forces GCAP in low-power standby mode.

	VRef
STBY High	Follows State of STVR
STBY Low	OFF

WCP has the ability to respond to interrupts during deep sleep therefore when in deep sleep the WCP will react to the insertion or removal of peripheral supplying power to the radio and/or the insertion or removal of the Headset jack (PHFA). Below is a table with the peripheral that will generate an interrupt.

Source	**Interrupt**
Ext B+	MOBPORTBI from GCAP to IRQ1 in WCP
Headset	TBD
Downlink	TBD

When camped and in deep sleep the WCP should wake up every 0.5seconds to read the A/D and perform a general check-update of the status of the radio.
Note that when the radio is supplied with External power (DHFA, Charger, CLA) the scanning rate should remain the same as the current software for the MC68338

5 WHITECAP RF INTERFACE
(Refer to MAGIC Contract Book 1.13 or 2.12)

5.0 Introduction

The MAGIC IC is intended to support the needs of the GSM/DCS1800 portable telephone products. **Kramer 400 MHz IF frequency, a 26 MHz crystal frequency, and the Pass 2 MAGIC IC. These changes will require MAGIC programming modifiecations over prior passes.**

Initially, for the P1 radio pass, the MAGIC Pass 1 IC will provide the first LO to the receiver at 710.2 to 744.8 MHz for EGSM with 215 MHz low side injection, and 795.1 to 832.4 MHz for DCS 1800 with low side injection . For the P2 and P3 radio pass, the IC will provide the first LO (RX VCO) to the receiver at 1140.2 to 1174.8 MHz for EGSM with 215 MHz high side injection, and 1590.2 to 1664.8 MHz for DCS 1800 with 215 MHz low side injection. An external RF mixer will convert the received signal to 215 MHz. The 215 MHz signal will then pass through an external SAW filter. The filtered signal will then enter the IC where it will be mixed with an internally generated 215 MHz signal to generate baseband I and Q signals. These baseband signals will then be filtered and amplified to provide RxI and Q. The RxI and Q signals will be converted into digital outputs and sent over a serial bus. The chip will provide for AGC control through the SPI bus.

For Kramer the MAGIC Pass2 IC will provide the first LO (RX VCO) to the receiver at 1325.2 to 1359.8 MHz for EGSM with 400 MHz high side injection, and 1405.2 to 1479.8 MHz for DCS 1800 with 400 MHz low side injection. An external RF mixer will convert the received signal to **400 MHz**. The 400 MHz signal will then pass through an external SAW filter. The filtered signal will then enter the IC where it will be mixed with an internally generated 400 MHz signal to generate baseband I and Q signals. These baseband signals will then be filtered and amplified to provide RxI and Q. The RxI and Q signals will be converted into digital outputs and sent over a serial bus. The chip will provide for AGC control through the SPI bus.

TX Data will be input serially. The present data bit and the three previous data bits will be used to set up one of 16 possible waveforms based on the sum of Gaussian pulses stored in a look up ROM. The resulting signal will then be clocked out at a 16X oversample rate. This data pattern will be input to a four accumulator fractional N synthesizer with 24 bit resolution. The synthesizer output will be 880.2 to 914.8 MHz for EGSM and 1710.2 to 1784.8 MHz for DCS 1800 with GMSK modulation and will be directly amplified to the transmitter output.

The reference oscillator will be a free running 13MHz crystal for MAGIC Pass 1, and 26 MHz for MAGIC Pass 2. AFC will be provided through the SPI bus as a programming offset to the fractional N division system. Resolution will be approximately 3Hz (6 Hz with Pass 2) with relative accuracy of less than 1Hz (2 Hz for Pass 2). Since the 13MHz or 26 MHz crystal will not be locked to the AFC, a second fractional divider system will be provided to derive an accurate 200kHz reference. This reference will then be multiplied in a PLL to 13MHz for use as an accurate clock to the logic sections of the radio. Since the crystal frequency changes, this divider will need to be programmed differently for Magic Pass 2.

Two tracking regulators will be provided to power the IC. A superfilter will also be provided to power the external main VCO.

Finally, an interface system of digital to analog converters will be provided to control the PAC IC. This will allow the logic sections of the radio to transmit data over SPI and then activate the transmitter with a single digital line as opposed to the present D/A output and saturation correction software.

5.1 Reference Oscillator

The reference oscillator will use a crystal at 13 MHz for MAGIC Pass 1 and 26 MHz for MAGIC Pass 2 with a stability over temperature of ± 20 ppm for GSM and ±11ppm for DCS 1800 to cover the camping requiremments in Kramer. An SPI controlled AFC is provided for by offsetting the fractional N division. Since an accurate clock is needed for the logic sections of the radio, a secondary fractional N division system is provided to derive an accurate low frequency clock. This low frequency clock is then multiplied up in the reference oscillator step up loop to an output frequency of 13MHz. The reference oscillator will be within 150ppm of 13MHz or 26MHz within 100msec of the REG_REF input rising to 2.775V.

The 13MHz reference will be provided externally for the logic sections as a CMOS output at 1Vp-p at CLK_OUT. The Logic clock will stay at 13 MHz for MAGIC Pass 1 or Pass 2 initially. This could change to 26 MHz in the future. **At power up, the crystal oscillator in the MAGIC Pass 1 IC will be routed directly to the CLK_OUT pin by pulling CLK_SEL low. For the MAGIC pass 2, the crystal oscillator divided by 2 will be routed to the CLK_OUT pin by pulling CLK_SEL low.** An SPI bit is then used to activate the digital AFC. Finally CLK_OUT is pulled high to route the output of the multiplied 200kHz reference to the CLK_OUT pin.

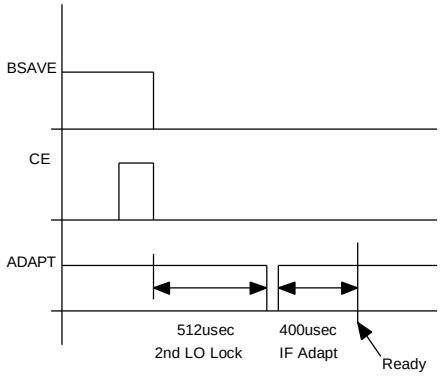
5.2 RX 2nd Local Oscillator

The 2nd LO VCO will be 430 MHz for both GSM and DCS-1800 in the P2 or P3 Kramer radio with the MAGIC Pass1 IC and **800 Mhz for Kramer with the MAGIC Pass2 IC.** The VCO frequency will be divided by 2 internal to the IC. Note that in the programming the factor of two is ignored so that if an IF frequency of 400MHz is desired, the programming is calculated as if the LO was at 400MHz even though it is actually at 800MHz.

5.3 Battery Save Operation

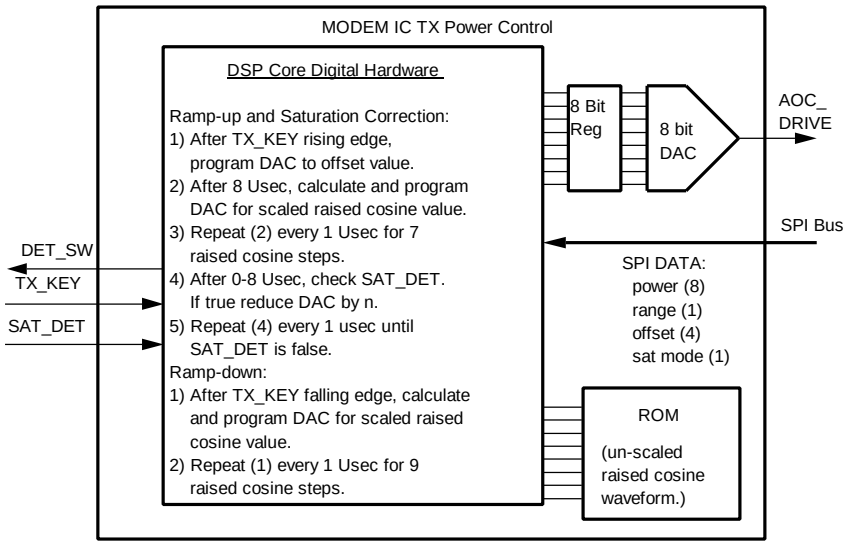
BSAVE (Bit 59 in the general control section of the SPI) is used for battery save. When BSAVE is programmed high then MAGIC will enter battery save mode on the falling edge of CE. Battery save will shut down the IF and main synthesizer. The tracking regulators will remain active but the superfilter will turn off. The IC will come out of battery save mode on the next falling edge of CE regardless of which SPI segment is programmed or the programmed state of BSAVE.

Recovery time from battery save must be less than 1mS. That is, the time from the falling edge of CE to the point where all VCO's are locked and all of the baseband circuits are settled must be no more than 1mS. MAGIC will output an internal adapt pulse 512usec after the CE which causes MAGIC to come out of BSAVE mode.

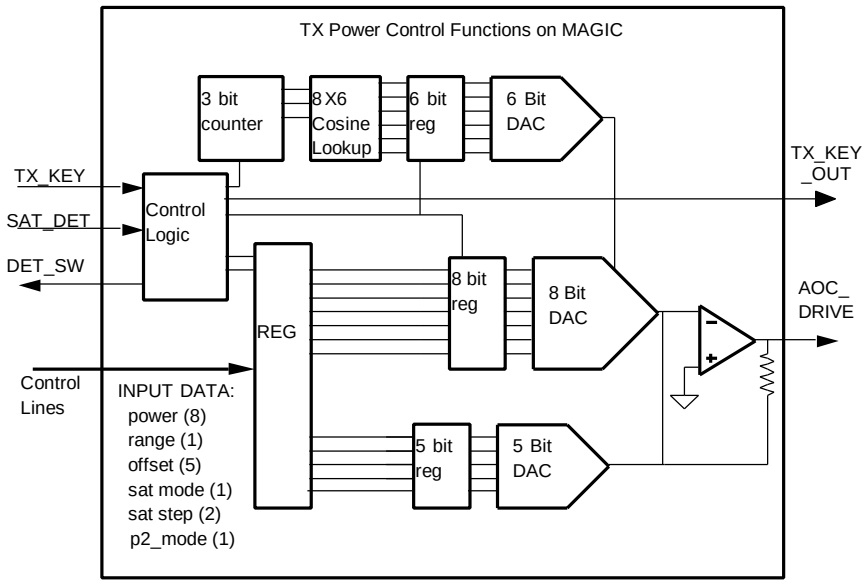


5.4 TX Power Control Operation

The IC will interface with the PAC IC to provide control of the output power and to form the correctly shaped ramp waveforms. The diagram below shows the operation of the present power control algorithm as implemented in the DSP.



MAGIC will perform the same function by using a combination of lookup tables, counters and D/As. In addition MAGIC will have added functionality for handling lower power outputs as will be required in phase 2 EGSM. This will alleviate some of the DSP computational burden and eliminate an analog interface to the DSP. A block diagram of this section is shown below.


TX Power Control Functions on MAGIC
3 bit counter
8 X6 Cosine Lookup
6 bit reg
6 Bit DAC
TX_KEY _OUT
TX_KEY
SAT_DET
DET_SW
Control Logic
REG
8 bit reg
8 Bit DAC
AOC_ DRIVE
Control Lines
INPUT DATA:
power (8)
range (1)
offset (5)
sat mode (1)
sat step (2)
p2_mode (1)
5 bit reg
5 Bit DAC

A description of the operation of this block is as follows.
Assume that P2_MODE is low.

Initialize

1) When TX_KEY goes high, program the 5 bit D/A to the 5 bit offset value (OFS0-4). The 8 bit D/A should be programmed to zero. The pin DET_SW is programmed to follow the state of SPI bit TXRNG. TX_KEY_OUT follows TX_KEY.

Ramp -Up

2) Eight usec after the rising edge of TX_KEY, program the 8 bit multiplying D/A to the 8 bit power setting (PWR0-7), and program the 6 bit D/A which drives the multiplication port of the 8 bit D/A to the first step of the raised cosine. The output of the 5 bit D/A and the 8 bit D/A are shown tied together. This is to indicate that the outputs will add.

3) Repeat step two 7 times on one usec intervals to output the rising 8 usec raised cosine by using consecutive values of the raised cosine lookup table to drive the 6 Bit D/A which drives the 8 bit multiplying D/A.

Saturation

4) For MAGIC Pass1, eighteen usec after the rising edge of TX_KEY (2 usec after the end of step 3) if SATMODE is high, then look at the state of SAT_DET. **For MAGIC Pass2, the time that SAT_DET is enabled is adjustable. After the rising edge of TX_KEY, wait for the number of counts stored in SAT_OFS. Then, if SATMODE is high, look at the state of SAT_DET.** For either pass, if SAT_DET is low then decrease the value of the 8 bit D/A by SAT_STEP.

5) Once the time has advanced to step 4) then if SATMODE is high and SAT_DET is low then decrease the 8 bit D/A by SAT_STEP on 1 usec intervals as long as TX_KEY is high. (If the value of the 8 bit D/A reaches zero then be sure any futher decrements result in a D/A program value of zero.)

Ramp-Down

6) On the falling edge of TX_KEY, program the 6 bit D/A which drives the multiplication port of the 8 bit D/A to the seventh step of the raised cosine.

7) Repeat step six 7 times on one usec intervals to output the falling 8 usec raised cosine by using consecutive values of the raised cosine lookup table read backwards to drive the 6 Bit D/A which drives the 8 bit multiplying D/A. At the end of this procedure the 8 bit D/A output should be zero.

8) **On the falling edge of DMCS, the 5 bit D/A is programmed to zero for the MAGIC Pass1 IC. The 5 bit D/A is programmed to zero right after step 7) for the MAGIC pass 2 IC. This will allow the offset D/A to drop to zero earlier in time to allow the radio Pout to get around the +28us time mask corner.**

If P2_MODE is high, then steps 1), 2), 3), 6), and 7) will change as follows.

Initialize

1) Four usec after TX_KEY goes high, program the 5 bit D/A to the 5 bit offset value (OFS0-4). The 8 bit D/A should be programmed to zero. The pin DET_SW is programmed to follow the state of SPI bit TXRNG. TX_KEY_OUT goes high 4 usec after TX_KEY goes high.

Ramp -Up

2) Twelve usec after the rising edge of TX_KEY, program the 8 bit multiplying D/A to the 8 bit power setting (PWR0-7), and program the 6 bit D/A which drives the multiplication port of the 8 bit D/A to the second step of the raised cosine. The output of the 4 bit D/A and the 8 bit D/A are shown tied together. This is to indicate that the outputs will add.

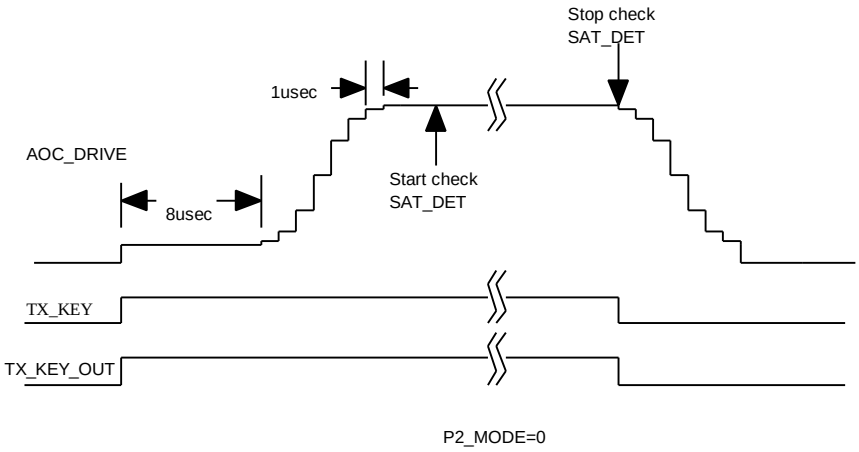
3) Repeat step two 3 times on one usec intervals to output the rising 4 usec raised cosine by using even numbered values of the raised cosine lookup table to drive the 6 Bit D/A which drives the 8 bit multiplying D/A.

Ramp-Down

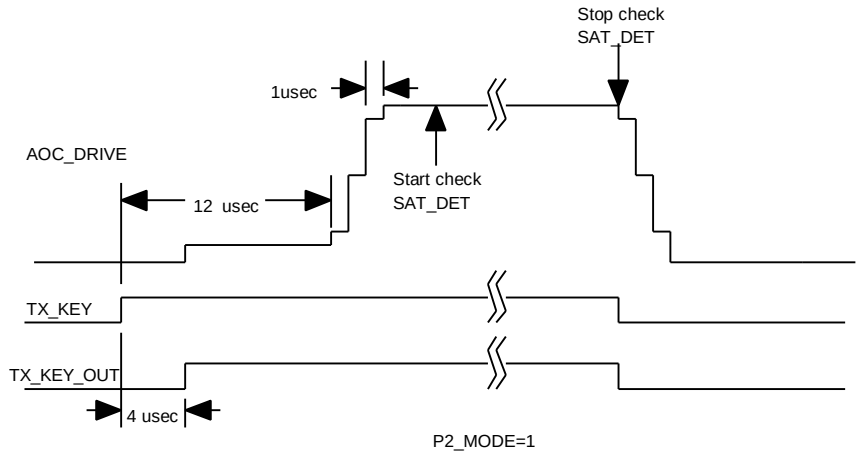
6) On the falling edge of TX_KEY, program the 6 bit D/A which drives the multiplication port of the 8 bit D/A to the sixth step of the raised cosine. TX_KEY_OUT goes low.

7) Repeat step six 3 times on one usec intervals to output the falling 4 usec raised cosine by using even numbered values of the raised cosine lookup table read backwards to drive the 6 Bit D/A which drives the 8 bit multiplying D/A. At the end of this procedure the 8 bit D/A output should be zero.

MAGIC Pass2 internal TX timing:

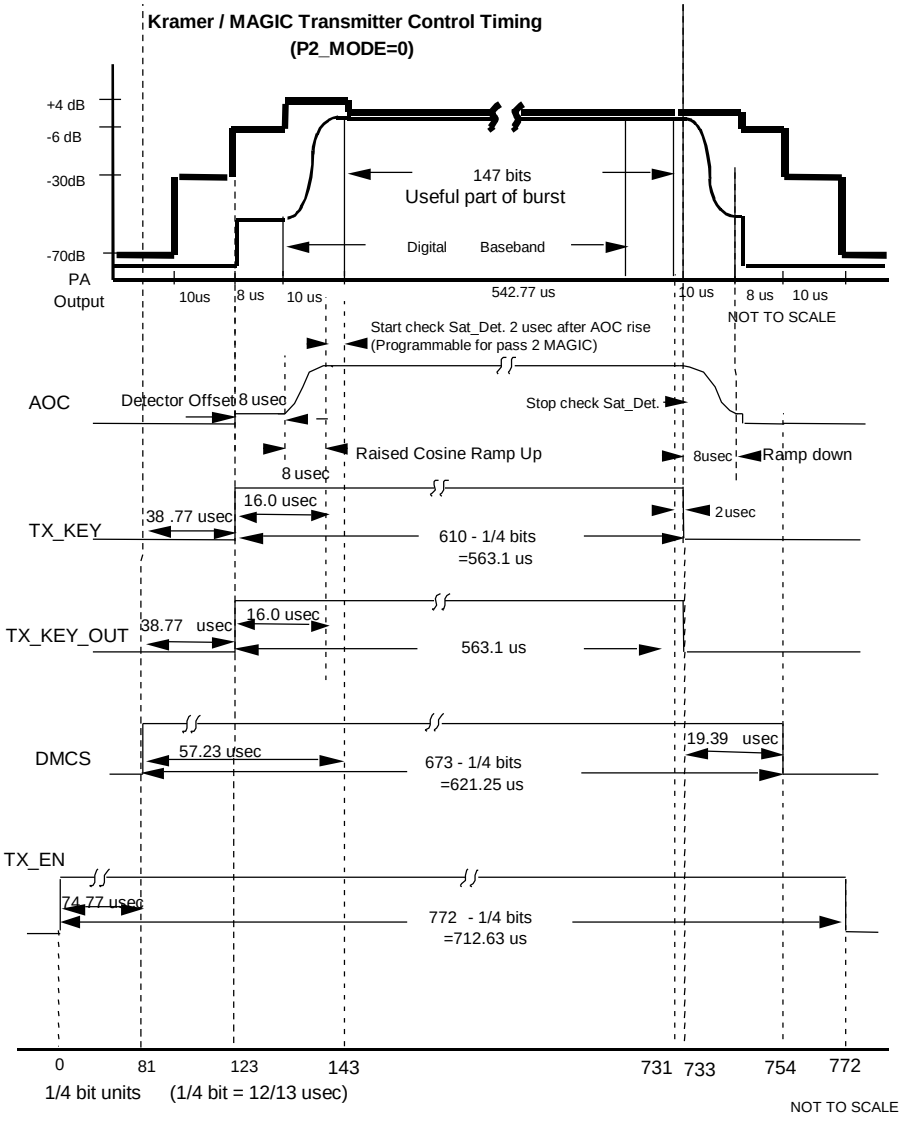


P2_MODE=0



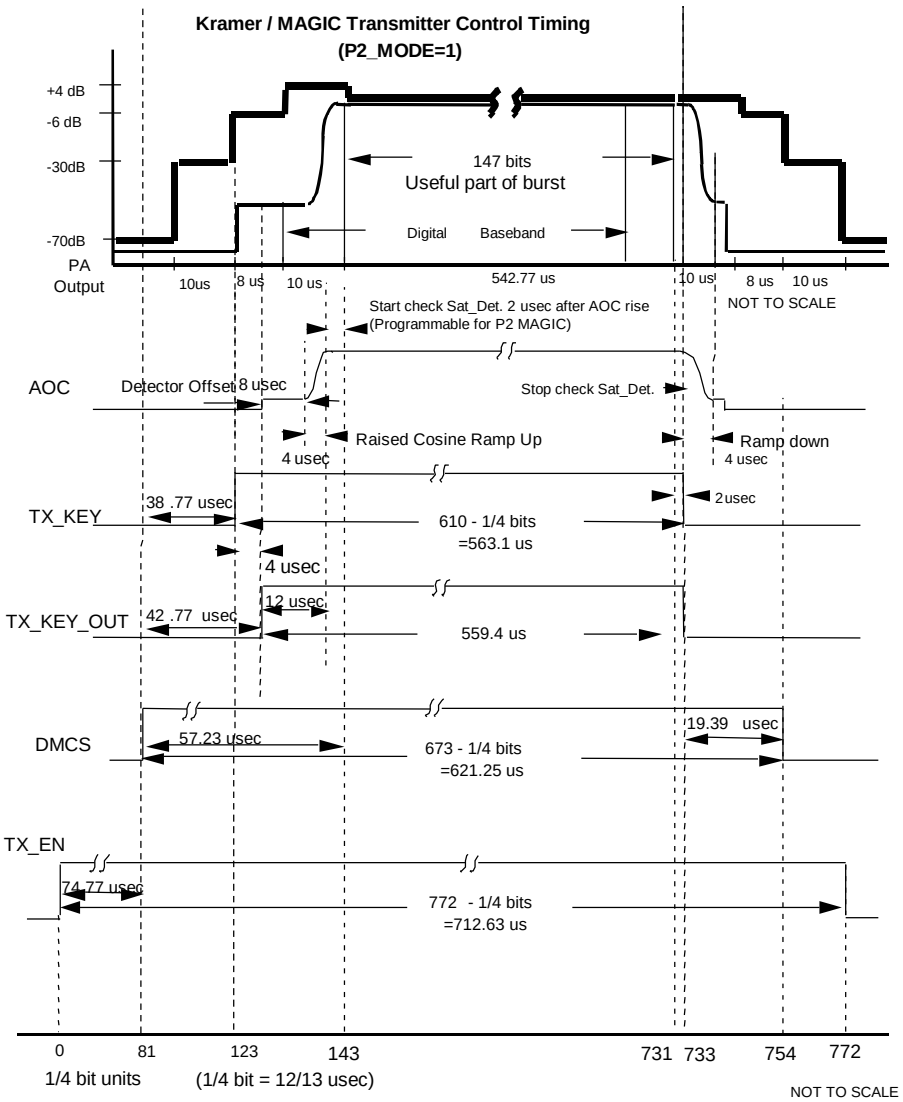
P2_MODE=1

Notes:
1) TX_KEY_OUT is a 0 to 2.775V CMOS output.
2) DET_SW is open drain. Therefore a logic high will result in a floating output.
3) SAT_DET is 0 to 2.775V TTL input.
4) The D/As must be monotonic. Integral non-linearity is 2 LSBs.
5) All D/As operate at a 1MHz rate.
6) The LSB of the 5 bit D/A is the same as the LSB of the 8 bit D/A at max output.
7) The maximum voltage out of AOC_DRIVE is approximately 1.9V.



Note: TX_KEY is set to give 2 usec of margin at the beginning and end of the burst. This will be optimized at a later date for type approval.

9/3 /97 GDL



Note: TX_KEY is set to give 2 usec of margin at the beginning and end of the burst. This will be optimized at a later date for type approval.

5.5 Power Supplies

The IC will contain 2 tracking regulators (external PNP or PMOS pass transistors) which will generate the supplies for the entire IC as well as the front end and the main VCO. A voltage of 2.775v must be provided to the REG_REF input. This pin has a maximum current draw of 200µA in mode. The reference voltage will be filtered and buffered for use on the IC. The buffered voltage should track the reference within ± 50mV. A raw supply voltage will be provided to the IC tracking regulators which will be at least 100mV above the reference (50mA output) and could be as high as 6.5Vdc.

A superfilter will be needed for the external VCO power supply. This superfilter, cascaded with the normal regulator and any filtering in front of the IC, will need to provide 80dB of rejection to a 0.1V step (risetime = 20µS) in the raw supply (battery). The superfilter will use an internal pass transistor that will be capable of driving a 45mA load with a voltage drop of less than 300mV relative to V2_OUT from the SF_OUT pin. An external .01µF cap will be required on SF_OUT.

All supplies within the IC must be within 5% of their final values after 10msec. The power on reset circuit contained within the crystal reference oscillator may be used to aid this functionality.

5.6 Logic Levels

Parameter	Conditions	Min	Max
Logic Input Low	Vcc<5V	0.3*REG_REF	
Logic Input High	Vcc<5V		0.7*REG_REF
Logic Output Low	Vcc<5V	0.3*REG_REF	
Logic Output High	Vcc<5V		0.7*REG_REF

5.7 RXI / RXQ Digital Baseband outputs

MAGIC will contain 8 bit successive approximation A/D converters which will derive a digital representation of the RxI and RxQ signals at a 1X or 2X sample rate. This converter will be activated if DA_EN is programmed high. **(Bit 55 for MAGIC pass1, bit 56 for MAGIC pass2 of the General Control Section of the IC).**

If DA_EN is high **(**which it will for Kramer), a serial bus consisting of SDFS, and SDRX will transmit the RxI and RxQ data in 2's compliment format. SDRX and SDFS are outputs from MAGIC. The clock used for the serial transfer will be SCLK_OUT. **This is the crystal reference oscilator divided to 13 Mhz at CMOS levels and is gated as needed for the data transfer.**

It is expected that data will be read on the falling edges of SCLK_OUT. The first valid data bit occurs on the next falling clock edge after SDFS goes high.

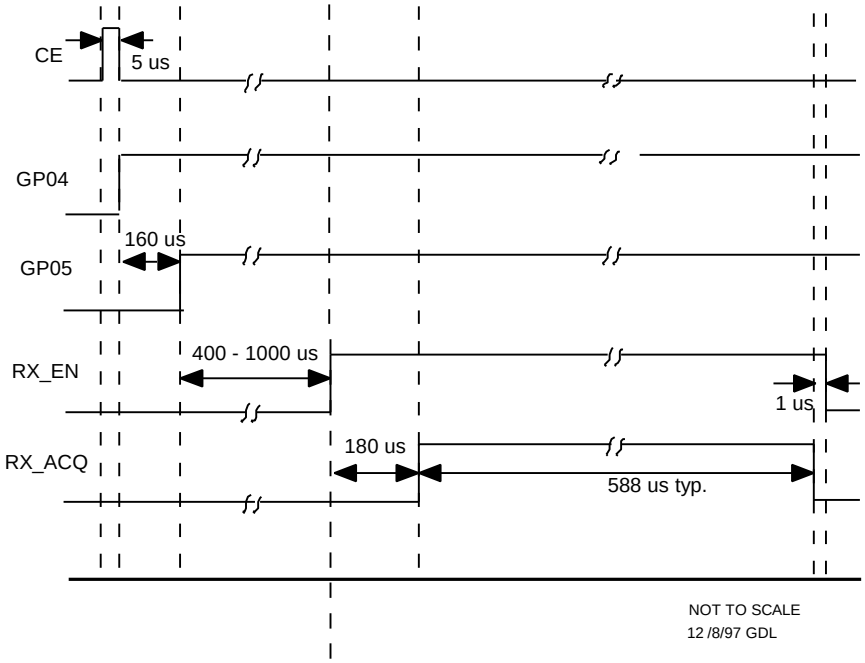
When RX_ACQ goes high, MAGIC will acquire an RxI and an RxQ sample after two periods of the reference clock. (13MHz). The data transmission over the serial bus will begin one period of SDFS after RX_ACQ has gone high. This will occur after 48 cycles of the reference clock (13MHz) or after 24 cycles of the reference clock if 2X sampling rate is selected. Since the first transition of SDFS is suppressed, valid data will be sent following every SDFS pulse.

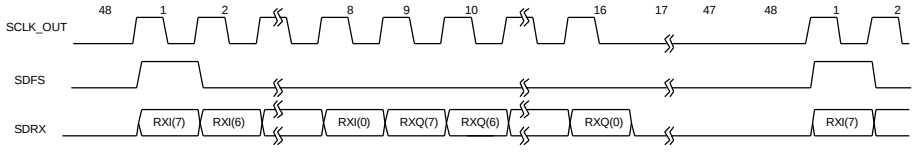
SCLK_OUT will be ported to the SCLK_OUT pin only as needed to transfer data. Therefore after each transfer of RxI and RxQ data, the SCLK_OUT pin will go low. If RX_ACQ goes low then SCLK_OUT, SDRX and SDFS will go low after completing the data transfer in progress. (i.e. the outputs will go low on the next normal occurance of SDFS.)

The format for 1X oversample mode data transmission will be 8 bits for the I channel, then 8 bits for the Q channel followed by 32 zeros. If 2X_EN (bit 61 of the IF section) is set high, indicating a 2X oversample mode, then the output sequence will be 8 bits for the I channel, 8 bits for the Q channel, 8 zeroes, 8 bits for the second I channel sample, 8 bits for the second Q channel sample followed by 8 zeros .

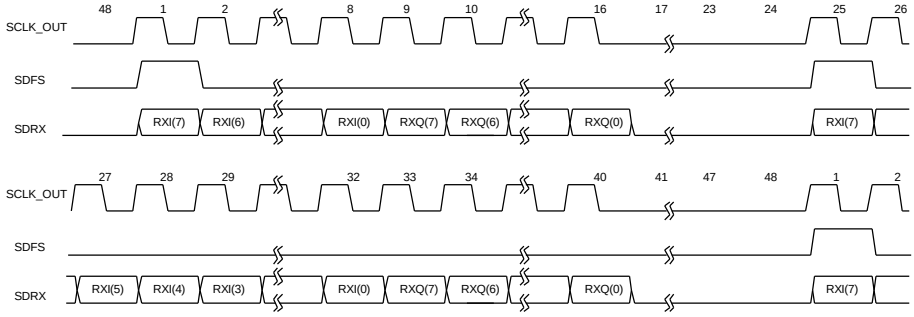
For Kramer, DA_EN should be programmed high.

Modulus 2 / MAGIC Receiver Timing





1X Sampling
RXI / RXQ Serial Interface



2X Sampling
RXI / RXQ Serial Interface

5.8 RXI / RXQ Analog Baseband outputs

If DA_EN is programmed low then all of the digital baseband interface is disabled and the analog RxI and RxQ output are available at TEST1 and TEST2.

The analog outputs will not be used for Kramer. DA_EN is programmed high to activate the digital baseband interface (A/D converter).

5.9 AGC

The IF agc is made up of 30dB to 120dB of linear range and a 25dB step attenuator. Both of these are controlled over the SPI bus.
The distribution and range of the AGC can be selected with the GDIST section of the SPI. See the IF programming section of the SPI description. Note that the
The AGC must be linear to within +/- 0.5db over a 20db range and must be linear within
+/-1.5db over the full range.

5.10 AFC

For the MAGIC Pass 2 IC and Kramer radio, use the following AFC information:

If AFC_DIG is programmed high then AFC is accomplished on the main synthesizer as a programming offset added to the main synthesizer division programming. 16 bits are used for the AFC offset. The offset is a two's compliment number. Two zeros are concatenated to the LSB of the AFC number. Thus the frequency offset of the main synthesizer will be $(AFC15,AFC14, ...AFC0,0,0)_B/2^{24}$*26MHz. The maximum AFC offset is ±203.122kHz =±((2^{17}-4)/2^{24}*26MHz)with a resolution of 6.1988 Hz (4/2^{24}*26MHz). It is assumed that the channel programming is offset by -203.122 kHz so that a two's compliment AFC setting of 0000_H is zero offset from the desired frequency.

The reference for the second LO of the IF section is derived from the 26MHz reference oscillator. Bits 41 through 47 (RIF0 - RIF6) of the general IC control section of SPI are used to program this divider. Nominal GSM setting will program this to 26.

Since the reference oscillator is not directly corrected by AFC, then any error in the 26MHz reference oscillator will be present on the second LO. When the DSP calculates the receive AFC correction to be programmed into the main synthesizer division ratio, it will actually be correcting for the sum of the second LO and the main synthesizer frequency .

Therefore the AFC setting during TX will be (f_{TX}/f_{RX})*(measured RX error) and the setting during RX will be the measured RX error. These two AFC values are programmed in two's compliment as AFC_T and AFC_R bits 0 through 15 and bits 16 through 31 of the AFC section of SPI. AFC_SEL (bit 32 of the Channel Select section of SPI) selects which AFC is applied to the next time slot.

The above setting will result in an accurate main synthesizer frequency but the crystal reference will not be precisely accurate. A secondary division system is provided to derive an accurate 200kHz internal signal.

The integer part of the secondary division is programmed with bits 32 through 39 (RN0 - RN7) of the AFC section of SPI. Nominal programming is 130 for GSM with a 26MHz crystal. The maximum division of the secondary division system will be 255.

The fractional division part of the secondary division system will be set by bits 40 through 61 (RAFC2 - RAFC23) of the AFC section of SPI. (A factor of 7 is also added due to the FN.)

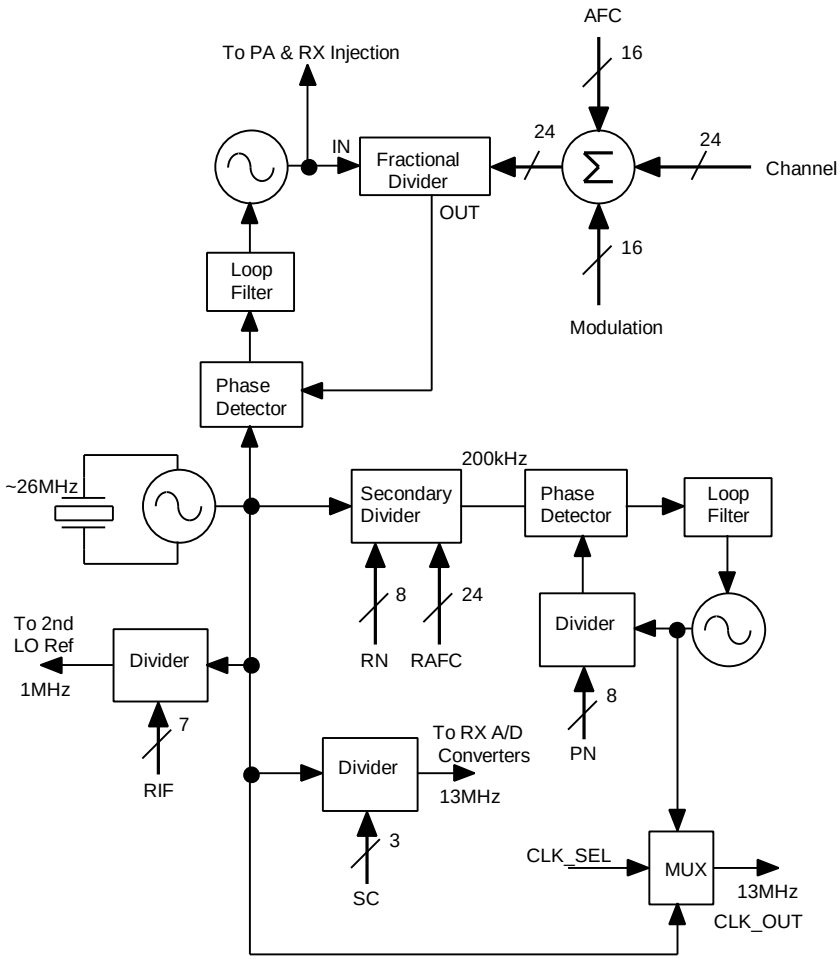
The total secondary division will thus be

$257-((RN[6:0])_B+ (RAFC[23:2], 0, 0)_B/2^{24}+7)$.

The accurate 200kHz clock will be used as the reference for an internal PLL system to derive a 13MHz output (CLK_OUT) to the digital circuitry external to MAGIC. Bits 33 through 40 (PN0 -PN7) of the general IC control section of SPI are used to program the multiplication factor. Nominal GSM setting will program this to 65.

Finally, the clock used for the RX serial interface is derived from CLK_OUT. Bits 53 through 55 (SC0 -SC2) of the general IC control section of SPI are used to program this divider. Nominal GSM setting will program this to 2.

The diagram shown below details the operation of the digital AFC system.



Given that the required main loop AFC offset has been determined, the secondary division is determined as follows: (Assuming a 26MHz crystal, 13MHz output, and a 200kHz internal reference.)

Let the main VCO frequency be f_{TX} and the total main loop division be N_t. N_t has been accurately adjusted by the AFC system. Then the frequency of the free-running crystal (f_M) may be determined as:

$f_M = f_{TX}/N_t$

Now add a second divider to the output of the free-running crystal oscillator with division ratio equal to N_2. Then the low frequency reference can be expressed as:

$f_{Ref} = f_M/N_2$

Combine these two equations to obtain the low frequency reference only as a function of the main VCO output.

$f_{Ref} = f_{TX}/(N_t*N_2)$

Based on this, the division ratio can be determined as follows:

1) Lock to any ARFCN (Actual Radio Frequency Channel Number)
For EGSM this results in f_{TX} = 880 + 0.2*(ARFCN) MHz after the AFC algorithm has adjusted N_t to lock on the channel.

2) Assume f_{Ref} = 200kHz (for example)
Then 0.2 = {880 + 0.2(ARFCN)}/(N_t*N_2)

3) Solve for N_2.
N_2 = 4400/N_t + ARFCN/N_t

For fractional N systems N_t =N*P+A+(Numerator$_{channel}$ + Numerator$_{AFC}$)/ Denominator.

--or--

N_2= f_{TX}/(N_t* f_{Ref})

But N_t = (f_{TX} + f_{AFCT})/(26MHz) thus (assuming f_{Ref} =200kHz)

N_2= (f_{TX} *26e6) / ((f_{TX} + f_{AFCT})*200e3)=130*(1/(1 + f_{AFCT}/ f_{TX})=130*(1/(1 + f_{AFCR}/ f_{RX})

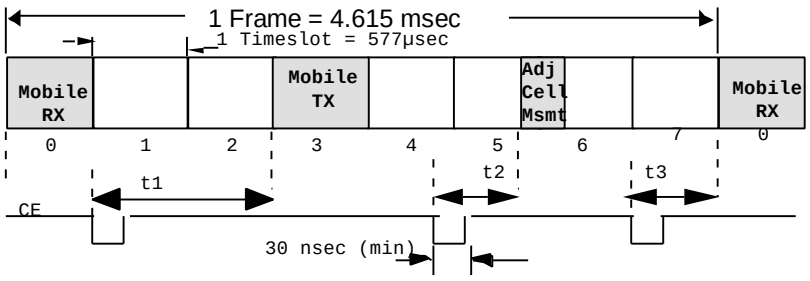
This initial programming will not change if the ARFCN is changed, since N_t will change with ARFCN to maintain N_2 constant. The only situation in which N_2 will need to change is if N_t is changed by the AFC algorithm.

If AFC_DIG is programmed low then the digital AFC system is powered down. If CLK_SEL is pulled low then the crystal oscillator output is tied to CLK_OUT. AFC is accomplished with an external 12 bit D/A driving a varactor diode to warp the crystal in this mode of operation. AFC_DIG should be programmed high to activate the digital AFC in Kramer.

At power up, CLK_SEL must be pulled low so that a valid clock is sent to the logic sections of the radio. The processor will then program the AFC system and set AFC_DIG high to set up the accurate digital clock. Finally the processor will pull CLK_SEL high and use the accurate digital clock.

5.11 CE

This input supplies the latch enable logic level **(Minimum pulse width low of six cycles of te reference oscillator for MAGIC Pass2)** for the SPI data. The falling edge of this signal therefore starts the frequency acquisition process of the desired channel if the channel or AFC SPI group is reprogrammed. A transition from high to low on this line latches in the data from the shift register. A logic high allows changing of the data in the shift registers without affecting the current programming.



The above diagram illustrates a typical traffic channel and the relationship of the required CE pulse to the MS RX timeslot if the channel or AFC SPI group is reprogrammed. Timing limits are:

t1: >200µS from the falling edge of CE to serving cell DMCS
t2: >400µS from the falling edge of CE to serving cell RX_ACQ
t3: >400µS from the falling edge of CE to adjacent cell RX_ACQ

5.12 ADAPT

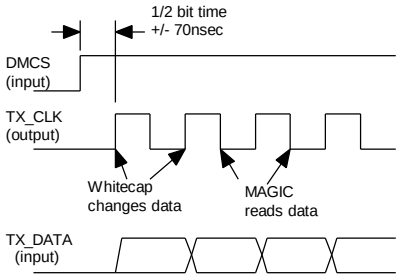
Adapt will occur on the falling edge of CE if ADAPT_EN (bit 58 of the General Control section of SPI) is set to a one. Timing requirements are as shown above for CE.

MAGIC will automatically pulse the adapt line 512usec after the occurance of the CE which causes MAGIC to come out of BSAVE mode. This assumes that the radio will always need to perform some sort of receive after coming out of battery save.

5.13 TX Data Transmission

MAGIC will contain a look-up ROM to trace out frequency versus time corresponding to GMSK modulation. The modulator will use the present data bit and the previous three data bits. MAGIC will perform the required differential encoding of the transmit data prior to transmission.

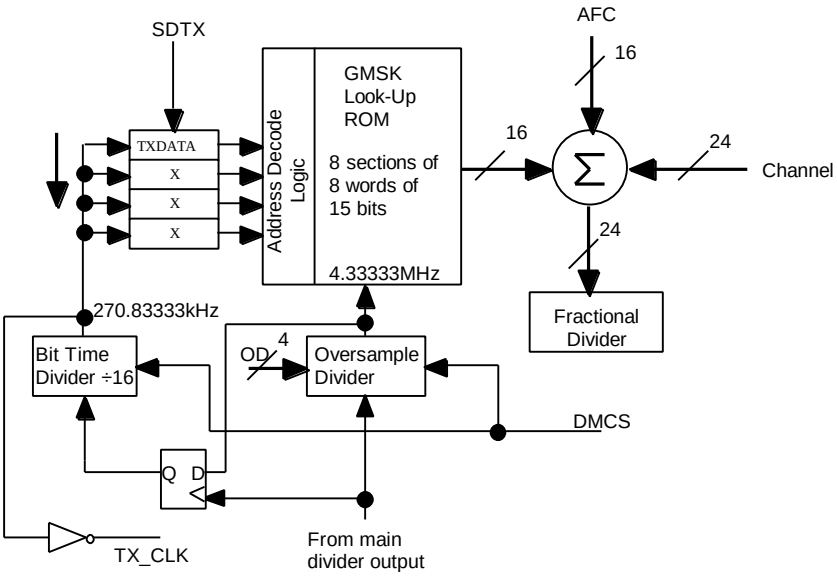
On the rising edge of DMCS, MAGIC will sample a TX data bit from the SDTX line. An additional TX data bit will be sampled from the SDTX line on every bit clock interval until DMCS goes low. DMCS is expected to have 1/4 bit time resolution to accurately set the starting time. The transmission of data to the power amplifier will be delayed by 9/13usec due to the fractional divider system. The bitclock within MAGIC will be synchronized to CLK_OUT with the phase set by the rising edge of DMCS. (SDTX cannot change within ±160nsec of the rising edge of the internal bit clock.) A gated bit clock will be provided at TX_CLK. This clock will be inverted from the internal bit clock. Thus when TX_CLK transitions from low to high, a new SDTX bit should be sent. MAGIC will read SDTX on the high to low transition of TX_CLK. TX_CLK will have 50% duty cycle. TX_CLK may be high or low before the rising edge of DMCS. The state will depend on the state of TX_CLK when DMCS went high to low on the previous burst.



The oversample divider is programmed with bits 47 through 50 (OD0 - OD3) of the general IC control section of SPI for MAGIC Pass 1 and bits 48 through 51 for MAGIC Pass 2. Nominal programming for GSM and DCS is 3.

The center frequency of the channel selection will be offset by -101.562kHz so that an output of 8000_H from the Look-Up ROM will correspond to a 0Hz offset.

The diagram below shows a block diagram of this structure.


SDTX
AFC
16
GMSK
Look-Up
ROM
8 sections of
8 words of
15 bits
4.33333MHz
Address Decode
Logic
TXDATA
X
X
X
16
24
Channel
24
Fractional
Divider
270.83333kHz
Bit Time
Divider ÷16
OD
4
Oversample
Divider
DMCS
Q
D
TX_CLK
From main
divider output

5.14 Programming Examples (from MAGIC Contract Book 2.12)

Programming Example with 153MHz IF

Assume the following conditions:

Desired ARFCN = 10 (F_{Main} = 892MHz)
Rx/Tx split = 45MHz
Low side RX injection
Measured AFC offset at the RX frequency of 937MHz = +1.05kHz
RX IF Frequency = 153MHz
Crystal Reference = approx 13MHz
CLK_OUT = 13MHz

During the receive time slot the main division will be (937MHz-153MHz- 203.125kHz)/13MHz = 60.29206731. The factor of 203.125kHz is due to the offset of the modulator and the AFC system. (This offset corresponds to a subtraction of 40000_H in the numerator programming. Thus it may be easier to ignore it at first and subtract it off after the calculation.) The integer part can be realized with **N=A_H** and **A=3**. This is N*5 + A +7 = 60 since the main loop uses a 5/6 prescaler. The fractional part can be realized as **NUM = $4AC4EC_H$**. The AFC correction in the receive time slot is -1.05kHz or **AFC_R = $3EAD_H$**.

During the transmit burst, the main division will be (892MHz -203.125kHz)/13MHz = 68.59975962. The integer part can be realized with **N = C_H** and **A =1.** The fractional part can be realized as **NUM = $9989D8_H$**. This is NUM/2^{24} = 0.59975964. Note that if the division had been initially calculated without the 203.125kHz offset then all would be the same except NUM would be 9D89D8.

Since it was assumed that there was an AFC error of +1.05kHz at the RX frequency, the AFC in the transmit burst will be set to offset the main loop by 1.05kHz*(892/937) = -1kHz. This is realized by programming **AFC_T = $3EBD_H$**. This is {AFC,0,0}/2^{24}* 13E6. Note that {AFC,0,0} means that the 16 bit AFC number is concatinated with two LSB zeros so that the LSB of AFC is 4 instead of 1.

Given this AFC error the division ratio for the accurate 200kHz reference can be calculated as follows:

The total loop division is $N_t = N*5 + A + 7 + (NUM + 40000_H)/ 2^{24} + \{AFC,0,0\}/2^{24}$

$N_t = 68 + 10324440/2^{24} - 1292/2^{24} = 68.615307569$

Therefore:

$200kHz = 892MHz/(68.615307569*N_2)$

$N_2 = 65.00007299$ This is realized as (257-RN) - {RAFC[23:2],0,0}/2^{24} -7 = N_2.

Thus **RN = $B8_H$** and **RAFC[23:2] = $3FFECC_H$** ({RAFC[23:2],0,0} = $FFFB37_H$).

If a new channel is selected RN and RAFC do not change. If AFC is updated then RN and RAFC will need to be modified to maintain the accurate 200kHz reference.

Assume that CLK_OUT is set to 13MHz then the rest of the programming is as follows (These numbers are fixed for the system and do not depend on channel or AFC):

PN = $C0_H$ (=257-65) to multiply 200kHz to 13MHz

RIF = 74_H (= 129-13) to divide the 13MHz crystal to 1MHz for the 2^{nd} LO reference

OD = E_H (= 17-3) to divide the main divider to 4.33333MHz for the oversample clock
SC = 4 (= 5-4) to set 13MHz for the RxI and Q A/D converters.

SN = EE_H (= 257-19) to set the second LO N counter.
SA = 7 (= 8-1) to set the second LO A counter.

If a 26MHz CLK_OUT was desired then the programming would be as follows:

PN = 82_H

Programming Example with 400MHz IF (POR default)
Assume the following conditions:

Desired ARFCN = 10 (F_{Main} = 892MHz)
Rx/Tx split = 45MHz
High side RX injection
Measured AFC offset at the RX frequency of 937MHz = -1.05kHz
RX IF Frequency = 400MHz
Crystal Reference = approx 26MHz
CLK_OUT = 13MHz

During the receive time slot the main division will be (937MHz+400MHz- 406.250kHz)/26MHz = 51.40745192. . The factor of 406.250kHz is due to the offset of the modulator and the AFC system. (This offset corresponds to a subtraction of 40000_H in the numerator programming.) The integer part can be realized with **N=8$_H$** and **A=4**. This is N*5 + A +7 = 51 since the main loop uses a 5/6 prescaler. The fractional part can be realized as **NUM = 684EC5$_H$**. The AFC correction in the receive time slot is +1.05kHz or **AFC$_R$ = 00A9$_H$**.

During the transmit burst, the main division will be (892MHz - 406.250kHz)/26MHz = 34.29206731. The integer part can be realized with **N = 5$_H$** and **A =2.** The fractional part can be realized as **NUM = 4AC4EC$_H$**. This is NUM/2^{24} = 0.29206731.

Since it was assumed that there was an AFC error of -1.05kHz at the RX frequency, the AFC in the transmit burst will be set to offset the main loop by 1.05kHz*(892/937) = +1kHz. This is realized by programming **AFC$_T$ = 0091$_H$**. This is {AFC,0,0}/2^{24}* 26E6. Note that {AFC,0,0} means that the 16 bit AFC number is concatinated with two LSB zeros so that the LSB of AFC is 4 instead of 1.

Given this AFC error the division ratio for the accurate 200kHz reference can be calculated as follows:

The total loop division is $N_t = N*5 + A + 7 + (NUM + 40000_H)/ 2^{24} + \{AFC,0,0\}/2^{24}$

$N_t = 34 + 5162220/2^{24} + 145/2^{24} = 34.307700932$

Therefore:

$200kHz = 892MHz/(34.307700932*N_2)$

$N_2 = 129.9999673$ This is realized as (257-RN) - {RAFC[23:2],0,0}/2^{24} -7.

Thus **RN = 78$_H$** and **RAFC[23:2] = 000089$_H$** ({RAFC[23:2],0,0} = 000224_H).

If a new channel is selected RN and RAFC do not change. If AFC is updated then RN and RAFC will need to be modified to maintain the accurate 200kHz reference.

Assume that CLK_OUT is set to 13MHz then the rest of the programming is as follows (These numbers are fixed for the system and do not depend on channel or AFC):

PN = C0$_H$ (=257-65) to multiply 200kHz to 13MHz

RIF = 67$_H$ (= 129-26) to divide the 26MHz crystal to 1MHz for the 2nd LO reference

OD = B$_H$ (= 17-6) to divide the main divider to 4.33333MHz for the oversample clock
SC = 3 (= 5-2) to set 13MHz for the RxI and Q A/D converters.

SN = CF$_H$ (= 257-50) to set the second LO N counter.
SA = 8 (= 8-0) to set the second LO A counter.

If a 39MHz CLK_OUT was desired then the programming would be as follows:

PN = C3$_H$

5.15 Magic / Whitecap MQSPI Interace

The following is the interconnection between MAGIC Pass 2and WHITECAP in Kramer:

Board Signal Name	**MAGIC ball**	MAGIC Pin Name	WHITECAP ball	WHITECAP Signal Name
DX1	**ball J3, input**	SPI_DATA	ball M7, output	DX1
MQSPI_CLK1	**ball H4, input**	SPI_CLK_SC_CLK4	ball M8, output	MQSPI_CLK1
MQSPI_CS1	**ball G5, input**	CE	ball L8, output	MQSPI_CS1
DR1			ball P5, output	DR1

DX1 (SPI_DATA): Serial Peripheral Interface Data, Data will be transmitted from WhiteCap to the MAGIC IC. Data will be latched into MAGIC either on rising edge or falling edge of clock depending on the control bit settings.
MQSPI_CLK : Clock used to shift data out serially.
MQSPI_CSI : Chip select signal used to latch data into MAGIC.
DR1 : Not connected to MAGIC

MAGIC will interface with the Serial Peripheral Interace 1 (SPI1) of the WHITECAP IC. Data on the bus will be changed on the fallling edge of the clock and sampled on the rising edge. The IC will only accept data if a valid chip select is given (active high) and data is latched in on the falling edge of MQSPI_CS1. There are 4 groups of SPI bits. Data is written most significant bit first. Each SPI transfer must consist of the full 64 bit field. Thus, additional dummy bits must be padded to those sequences which are not full length. The two most significant bits are used to select which SPI group is addressed.

The clock frequency can be set by writing to the SPI Default Register (SDEF). This register controls the default setups of SPI1 and SPI2. Registers with a 1 in their name refer to SPI1 while registers with a 2 in their name refer to SPI2.

SDEF	R/W @ $06h							
Bits 15-12	Bits 11-9	Bit 8	Bit 7	Bit 6	Bits 5-3	Bit 2	Bit 1	Bit 0
CSPL[3:0]	CBR1[2:0]	CPOL1	DIPH1	DOPH1	CBR2[2:0]	CPOL2	DIPH2	DOPH2
Default: 0000	000	0	0	0	000	0	0	0

CSPL[3:0] - Chip Select Polarity (one bit for each pin)
0 = Chip select will go high to start a transfer, and low to end a transfer.
1 = Chip select will go low to start a transfer, and high to end a transfer.

CSPL selects the phase of each chip select pin. Bit 3 corresponds to chip select 3, bit 2 to chip select 2, bit 1 to chip select 1, and bit 0 to chip select 0.

CBR[2:0] - Clock Baud Rate
Selects the clock frequency of the SPI. Selectable frequencies and corresponding bit representation are shown below.

Table X. SPI Selectable Clock Frequencies.

CBR[2:0]	**CLK Frequency**
000	13.00 Mhz
001	6.50 Mhz
010	3.25 Mhz
011	1.62 Mhz

100	812 Khz
101	406 Khz
110	203 Khz
111	101 Khz

CPOL - Clock Polarity
0 = The inactive state value of CK is low.
1 = The inactive state value of CK is high.

DIPH - Data In Phase
0 = Data In (DI) is changed on the falling edge of CK and captured on the rising edge of CK.
1 = Data In (DI) is changed on the rising edge of CK and captured on the falling edge of CK.

DOPH - Data Out Phase
0 = Data Out (DO) is changed on the falling edge of CK and captured on the rising edge CK.
1 = Data Out (DO) is changed on the rising edge of CK and captured on the falling edge CK.

MAGIC contains 4 groups of 64 bits that are programmable. Bit 64 and Bit 63 indicate which group is being addressed.

For the MAGIC Pass 2 IC to be used in Kramer:

Group 1 (IF Control) (program at power up)

Bit 63	Bit 62	.....	Bits 44:41	Bit 40	Bit 39	.....	Bit 1	Bit 0
0	0	.....			0	0.....0	0	0

Bits 39:0 are padded with 0s.

Bit 40: IF_HIGH. Program high for IF operation over 200MHz. When active, this bit increases the preamp load resistor to give the preamp 2dB more gain. Also when high the IF down conversion mixers are biased at a slightly higher current.
Program this bit to 1 for Kramer.with a 400 Mhz IF.

Bit 41 - 44: GDIST0 - GDIST3, AGC distribution and total range

SPI(44..41)	Preamp AGC	Baseband AGC	Total
0000	60dB	30dB	90dB
0001	60dB	60dB	120dB
0010	60dB	15dB	75dB
0011	60dB	45dB	105dB
0100	30dB	30dB	60dB
0101	30dB	60dB	90dB
0110	30dB	15dB	45dB
0111	30dB	45dB	75dB
1000	45dB	30dB	75dB
1001	45dB	60dB	105dB

1010	45dB	15dB	60dB
1011	45dB	45dB	90dB
1100	15dB	30dB	45dB
1101	15dB	60dB	75dB
1110	15dB	15dB	30dB
1111	15dB	45dB	60dB

Program bits 41 - 44 to 0101 for 90 dB total gain in Kramer

Bit 45 - 48: BW0 - BW3, IF bandwidth select.

Bit 48	Bit 47	Bit 46	Bit 45	3 dB Bandwidth
0	0	0	0	60.0 kHz
0	0	0	1	62.2 kHz
0	0	1	0	66.5 kHz
0	0	1	1	73.0 kHz
0	1	0	0	81.6 kHz
0	1	0	1	92.2 kHz
0	1	1	0	105.1 kHz
0	1	1	1	120.0 kHz

Program bits 48 - 45 to 0011 for a 73 kHz 3 dB bandwidth for Kramer

Bit 49 - 52: SA0 - SA3, the second LO A counter, program (8-A(desired)).
Program bits 52 - 49 to 1000 for a 2nd LO counter = 8 for Kramer.

Bit 53 - 60: SN0 - SN7, the second LO N counter, program (257-N(desired)).
Program bits 60 - 53 to 11001111 for a 2nd LO Counter = 207 for Kramer.

Bit 61: 2X_EN Program high for 2X oversample on receive. Program low for 1X.

Bit 62: Logic 0.

Bit 63: Logic 0.

Group 2 (General Control)

Bit 63	Bit 62	.....	Bit 13	Bit 12	Bit 11	.....	Bit 1	Bit 0
0	1	.....			0	0.....0	0	0

Bits 11:0 are padded with 0s.

Bit 12: DA_CTL, A/D control transfer. If this bit is programmed low then the A/D is controlled by the state of DA_EN. If this bit is programmed high then if DA_EN is high and if AFC_SEL is low then the A/D is enabled. This will allow the A/D to turn off during TX times without an additional SPI write.

Bit 13: COB_SEL, Clock Output Bandwidth select. If programmed high the clock output buffer bandwidth is set for 26MHz. If low then it is set for 13MHz. (POR default is high)
This bit should be set to 0 for Kramer with a 13 Mhz Logic clock.

Bit 14: XD2, if programmed to 1 then the crystal reference is divided by 2 before being applied to CLK_OUT if CLK_SEL is set low. If low then divide

by one. (POR default is high)
This bit should be set to 1 for Kramer.

Bit 15: BI_TX, if programmed to 1 then the second LO of MAGIC will enter battery save mode when afc_sel is high. (TX mode)
This bit should be programmed to 0 for Kramer.

Bit 16: MOD_INV, if programmed to 1 the output of the modulation differential encoder will be as in Pass 1. If programmed to a zero then the output will be inverted.
This bit should be programmed to 1 for Kramer.

Bit 17: MOD13_26B, if programmed to 0 modulation will be correct for use with a 26MHz crystal reference, if programmed to 1 the modulation will be correct for use with a 13MHz crystal reference.
This bit should be programmed to 0 for Kramer.

Bit 18: MNCP_INV, if programmed to 0 the charge pump will source current to increase frequency, if programmed to one the charge pump will sink current to increase frequency.
This bit should be programmed to 0 for Kramer.

Bit 19 -20: SAT_STEP, selects the number of D/A LSBs which will be stepped during each time interval during saturation correction.
These bits should be read from the PA table as needed for Kramer.

Bit 21 - 24: SAT_OFS0 - SAT_OFS3 the programming input for the number of microseconds by which the start of saturation detection is delayed from the end of the ramp up of the power control.
Bits 24 - 21 should be programmed to 0100 for a 4 microsecond delay after the AOC rise ends for Kramer as the TX timing has been defined in this document. Bit 24 - 21 will be programmed to 0010 for a 2 microsecond delay after the 2 microsecond timing advance on AOC has been removed once a call is established.

Bit 25 - 29: TMUX0 -TMUX4, Test mux control bits.

	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	TEST1	TEST2
0	0	0	0	0	0	GND	GND
1	0	0	0	0	1	GND	VCC
2	0	0	0	1	0	VCC	GND
3	0	0	0	1	1	VCC	VCC
4	0	0	1	0	0	FVMAIN	MAIN_FR
5	0	0	1	0	1	GND	GND
6	0	0	1	1	0	ADAPT1	ADAPT2
7	0	0	1	1	1	ADAPT3	ADAPT4
8	0	1	0	0	0	LO2_FR	LO2_FV
9	0	1	0	0	1	LO2_UP	LO2_DN
10	0	1	0	1	0	POR	unused
11	0	1	0	1	1	FV13PLL	FR13PLL
12	0	1	1	0	0	unused	
13	0	1	1	0	1	unused	
14	0	1	1	1	0	unused	
15	0	1	1	1	1	GPO4	GPO5
16	1	0	0	0	0	OTA	OTAIN
17	1	0	0	0	1	TRKVCO	VLOOP

18	1	0	0	1	0	IF_AGC	GND
19	1	0	0	1	1	RXI_IN	RXQ_IN
20	1	0	1	0	0	I_MON	Q_MON
21	1	0	1	0	1	BBI_IN	BBI_OUT
22	1	0	1	1	0	BBQ_IN	BBQ_OUT
23	1	0	1	1	1	MIXOUTI	MIXOUTQ
24	1	1	0	0	0	VAGI	VAGQ
25	1	1	0	0	1	RXI	RXQ
26	1	1	0	1	0	unused	
27	1	1	0	1	1	unused	
28	1	1	1	0	0	unused	
29	1	1	1	0	1	unused	
30	1	1	1	1	0	unused	
31	1	1	1	1	1	unused	

Bits 29 to 25 should be set to 01111 for Kramer to enable the GPO4, GPO5 output at the Test1 and Test2 pins for RX VCO turn on / off control.

Bit 30 - 32: CPTEST0 - CPTEST2. If CPTEST0 is low the charge pumps have normal operation. If CPTEST0 is high, a one in CPTEST1 causes all charge pump outputs to source current. If CPTEST0 is high, a one in CPTEST2 causes all charge pump outputs to sink current.
Bits 30 to 32 should be set to 000 for Kramer.

Bit 33 - 40: PN0 - PN7 the programming input for the multiplication factor from the accurate low frequency reference to CLK_OUT. Program as 257-desired value.
Bits 40 - 33 should be programmed to 11000000 for PN = 192 for Kramer.

Bit 41 - 47: RIF0 - RIF6 the programming input for the division factor from the reference oscillator to the reference for the second LO of the IF. Program as 129 - desired value.
Bits 47 - 41 should be set to 1100111 to program RIF to 103 for Kramer.

Bit 48 - 51: OD0 - OD3 the programming input for the division factor from the output of the main divider to the oversample clock input of the modulator. Program as 17 - desired value.
Bits 51 - 48 should be programmed to 1011 to program OD to 11 for Kramer.

Bit 52: 2X_SEL if programmed low then TXRNG (SPI Group 3 bit 50) is routed to the A/D converter to control the selection of 1X versus 2X oversampling. (TXRNG will still also be connected to DET_SW as described in Group 3)
If programmed high, then EN_2X (SPI Group 1 bit 61) is routed to the A/D converter to control the selection of 1X versus 2X oversampling as described in Group 1. POR default is low.

Bit 53 - 55: SC0 - SC2 the programming input for the division factor from the crystal reference oscillator to the internal 13MHz clock for the RX serial interface. Program as 5 - desired value.
Bits 55 - 53 should be programmed to 011 to program SC to 3 for Kramer.

Bit 56: DA_EN Program high to activate the A/D converter and digital SDFS, SDRX, and SCLK_OUT outputs. Program low to de-activate the A/D converter and corresponding outputs. Control can be moved to AFC_SEL with DA_CTL.
This bit should be programmed to 1 for Kramer.

Bit 57: AFC_DIG Program high to activate the digital AFC system. Program low to power down the digital AFC sections.
This bit should be programmed to 1 for Kramer.

Bit 58: ADAPT_EN Program high to adapt on the falling edge of CE.
This bit should be programmed to 1 for Kramer.

Bit 59: BSAVE Program low for normal operation.
If BSAVE is programmed high then when CE transitions low, the IC will go into power save mode. In this mode only the reference oscillator and tracking regulators are active.
BSAVE will revert to a logic low on the next CE transition from high to low, regardless of which SPI segment is programmed.

Bit 60: ACC2 Program low for normal operation. If programmed high then the main fractional divider will be two accumulators instead of four.
This bit should be programned to 0 for Kramer.

Bit 61: ACC3 Program low for normal operation. If programmed high then the main fractional divider will be three accumulators instead of four.
This bit should be programmed to 0 for Kramer.

Bit 62: Logic 1.

Bit 63: Logic 0.

Group 3 (Channel Select)

Bit 63	Bit 62	Bit 61	.....	Bit 23	.....	Bit 0
1	0	Desense	.....	NUM23	.....	NUM0

Bit 0 - 23: NUM0 to NUM23 the numerator for the 24bit fractional N divider system. (The denominator is fixed at 2^{24} = 16,777,216)

Bit 24 - 26: A0 - A2 the programming input for the main loop A counter. Program as A desired.

Bit 27 - 31: N0 - N4 the programming input for the main loop N counter. Program as N desired.

Bit 32 AFC_SEL selects AFC_R and activates CP_RX if programmed to 0 and selects AFC_T and activates CP_TX if programmed to 1.

Bit 33: IFATT, IF step attenuator. Program low to disable the attenuator, program high to insert a 25dB pad at the input of the IF preamp.

Bit 34 - 41: AGC0 - AGC7, IF gain control bits. Program 0 for max gain and program 255 for maximum gain reduction.

Bit 42 - 49: PWR0 - PWR7, the phased D/A programming value corresponding to the power output levels.
These values should be obtained from the PA table for the appropriate band for Kramer.

Bit 50: TXRNG, selects the high or low range for the Power Amplifier Control IC. The state of DET_SW will follow this bit.
This value should be obtained from the PA table for the appropriate band for Kramer.

Bit 51 - 55: OFS0 - OFS4, phased value of offset voltage for Power Amplifier Control IC detector.
These values should be obtained as needed from the PA table for the appropriate band for Kramer. The technique that is used on the 8900 should be used to calculate the offset to be used for a given power step.

Bit 56: SATMODE,a high enables saturation detection and correction, low disables this function.
This value should be obtained from the PA table for the appropriate band for Kramer.

Bit 57: P2_MODE, if p2_mode is high then TX_KEY_OUT is delayed by 4 usec and the ramp is shortened from 8usec to 4usec. This is to be used in the low output power levels of GSM and DCS1800 phase 2.
NOTE: This bit should be set based on a flex threshold. Default for this threshold should be 16 (P2_MODE high for steps 16→19) for GSM and 11 for DCS (P2_MODE high for steps 11→15). The threshold should be flexible to any power step.

Bit 58: GPO1, the pin labeled GPO1 follows the programming of this bit.
This pin is not currently used in KRAMER.

Bit 59: GPO2, the pin labeled GPO2 follows the programming of this bit.
This pin will be used for band select between GSM and DCS 1800 in Kramer. Program to 0 to select GSM and to 1 to select DCS1800.

Bit 60: GPO3, the pin labeled GPO3 follows the programming of this bit.
This pin is not currently used in Kramer.

Bit 61: GPO4, TEST1 will follow the sense of this SPI bit if TMUX=01111. TEST2 will follow the sense of this SPI bit, delayed by 160usec from the falling edge of the CE which latches in this bit, if TMUX=01111.
GPO5 at the Test 2 pin will be used to turn on the RX VCO before RX_Enable goes high in Kramer.
This bit should be set to 1 with each RX adapt and RX time slot, and to 0 as soon as possible after the RX time slot has ended.

Bit 62: Logic 0.

Bit 63: Logic 1.

Group 4 (AFC)

Bit 63	Bit 62	Bits 61:40	Bits 39:32	Bits 31:16	Bits 15:0
1	1	RAFC23-RAFC2	RN7-RN0	AFCR15-AFCR0	AFCT15-AFCT0

Bit 0 - 15: AFCT0 - AFCT15 the AFC offset to the main loop divider in transmit mode.

Bit 16 - 31: AFCR0 - AFCR15 the AFC offset to the main loop divider in receive mode.

Bit 32- 39: RN0 - RN7 the whole part of the accurate reference fractional N divider. Program as 257 - desired value.

Bit 40 - 61: RAFC2 - RAFC23 the numerator of the accurate reference fractional N divider. (The denominator is fixed at 2^{24} = 16,777,216 and the two LSBs of the numerator are fixed at zero.)

Bit 62: Logic 1.

Bit 63: Logic 1.

5.16 Power On Reset (POR) of SPI

For MAGIC Pass 2, the POR is as follows:

Upon application of initial power to the IC the following SPI bits will be set up. The POR signal is taken from the crystal oscillator startup circuit. (all values are hex)

Group	Value	Group	Value	Group	Value
ifhigh	1	gdist	0	bw	3
sa	8	sn	CF	2x_en	0
da_ctl	0	cob_sel	1	2x_sel	0
xd2	1	bi_tx	0	mod_inv	0
mod13_26b	0	mncp_inv	0	sat_step	1
sat_ofs	0	tmux	0	cptest	0
pn	C0	rif	67	od	B
sc	3	da_en	1	afc_dig	1
adapt_en	1	bsave	0	acc2	0
acc3	0	NUM	4AC4EC	A	2
N	05	afc_sel	1	ifatt	0
agc	0	pwr	80	txrng	0
ofs	10	satmode	1	p2_mode	0
GPO1	0	GPO2	1	GPO3	0
GPO4	1	AFCT	0	AFCR	0
rn	78	rafc	0		

This will set up a maximum gain 400MHz IF, set the main synthesizer to 892MHz, and set up the AFC for a nominal 13MHz clock with a 26MHz crystal reference.

5.17 MAGIC / WHITCAP Interface

The following is the interconnection between MAGIC Pass 2and WHITECAP in Kramer:

Transmit

Board Signal Name	MAGIC ball	MAGIC Ball Name	WHITECAP ball	WHITECAP Signal Name
TX_KEY	**ball H5, input**	TX_KEY	ball E4, output	TIMING3
DM_CS	**ball J4, input**	DMCS	ball F5, output	TIMING4
BDX	**ball J2, input**	SDTX	ball C6, output	BDX
BCLKX	**ball G7, input**	TX_CLK_TEST_S01	ball A2, output	BCLKX
BCLKR	**ball F7,output**	SCLK_OUT	ball A3, input	BCLKR
RX_ACQ	**ball H8, input**	RX_ACQ_TEST_SI4	ball E3, output	TIMING1
BFSR	**ballG9, output**	SDFS	ball B4, input	BFSR
BDR	**ballG8, output**	SDRX	ball C4, input	BDR

TX_KEY: Digital input from the WHITECAP to the MAGIC to start / stop the PA control sequence. This signal should rise 114 uS after TX_EN and 39 uS after DM_CS, and fall 36 uS before the 713 uS long TX_EN.

DM_CS: Digital input from the WHITECAP to the MAGIC that starts the TX moduluation. This signal should rise 75 uS after TX_EN and fall 17 uS before TX_EN falls.

BDX (SDTX): Serial data in to the MAGIC TX modulator from the WHITECAP.

BCLKX (TX_CLK): Bit clock input to MAGICfrom WHITECAP for SDTX data transfer.

BCLKR (SCLK_OUT): Gated CMOS version of CLK_OUT from MAGIC to WHITECAP.
CLK_OUT is the 13 MHz clock output to digital circuitry in the radio.
SCK_OUT is at CMOS levels and is gated as needed for data transfer..

RX_ACQ: Serial bus enable used for receive functions to aquire RXI and RXQ data from the digital baseband interface in MAGIC. Used with SDFS and SDRX.

BFSR (SDFS): Framing signal for the serial bus to obtain receive data from the digital baseband interface in MAGIC.

BDR (SDRX): Serial data out of MAGIC for RX I and RXQ data from the digital baseband interface.

5.18 MAGIC / PAC Interface

The following is the interconnection between MAGIC Pass 2 and the PAC IC in Kramer:

Board Signal Name	**MAGIC ball**	MAGIC Ball Name	PAC IC pin	PAC IC Signal Name
TX_KEY_OUT	ball C5, output	TX_KEY_OUT	ball 10, input	TX_KEY
DET_SW	ball A5, output	DET_SW	ball 11, input	DET_SW
SAT_DETECT	ball B4, input	SAT_DET	ball 12, output	SAT_DET
AOC_DRIVE	ball B6, output	AOC_DRIVE_TEST_SI3	ball 8, input ball 9, input	AOC ACT

TX_KEY_OUT: Conditioned TX_KEY to the PAC IC. TX_KEY starts/stops the PA control sequence.

DET_SW: Output to the PAC IC power range input (open drain)

SAT_DET: Input from the PAC IC indicating PA saturation.

AOC_DRIVE: Output to the PAC IC drive input and activity detector.

5.19 MAGIC / FIRM IC Interface

The FIRM IC will not be used with the first several Kramer board passes. **In future board passes, the FIRM IC will be controlled with the GPO2 band select line and bit.**

5.20 MAGIC / TX VCO Interface

For MAGIC Pass 2 in Kramer:

The TX VCO band select will occur with a combination of DCS_SEL (GPO2) and PAC_EN. PAC_EN uses SF_OUT as a reference. PAC_EN is selected during TX mode by AND'ing SF_OUT with TX_EN. PAC_EN is then routed to one of the TX VCO's by DCS_SEL or GSM_SEL, an inverted versio of DCS_SEL. To select GSM TX Mode, DCS_SEL is set low to turn on the GSM TX VCO. At the same time, GSM_SEL turns off the DCS TXVCO. To select DCS1800 TX mode, DCS_SEL is set high to turn off the GSM TX VCO. At the same time, GSM_SEL turns on the DCS TX VCO

DCS_SEL (GPO2, ball C4):
This pin is low in GSM mode and high in DCS1800 mode for either a TX or RX function.

SF_OUT (ball C1): Super filter output (45mA max.). Switched to bias the base and emiiter of the TX VCO's with a clean supply.

CP_TX (ball B1): Charge pump output for the TX VCO's. The phase detector current is 5 mA.

PRSC_IN (ball A3): Main LO and TXVCO prescaler input. Usable up to 2 Ghz. The input level should be between -10dBm and 0 dBm. The input impedance will be approximatley 500 ohm // 2 pF plus package parasitics.

5.21 MAGIC / RX VCO Interface

For the MAGIC Pass 2 IC with Kramer

The RX VCO has a SF_OUT collector bias and is turned on at the base in the receive mode by the GPO5 (Test2) pin, which is delayed by 160uS from the falling edge of CE and the GPO4 pin at Test1. There is a single RX VCO. Band select is accomplished by switching on a pin diode in DCS1800 mode to reduce the inductance in the VCO. The control line to do this switching is called RX_DCS_GSM. It is derived from GPO5 and DCS_SEL. RX_DCS_GSM is at -5V in GSM RX mode and 2.75 V in DCS RX mode

DCS_SEL (GPO2, pin C4):
This pin is low in GSM mode and high in DCS1800 mode for either a TX or RX function.

GPO5 (Test2, pin 55):
This pin is set high to turn on the RX VCO before RX_EN and set low to turn off the RX VCO after RX_EN and RX_ACQ go low.

SF_OUT (pin 21): Super filter output (45mA max.)

CP_RX (pin 17): Charge pump output for the RX VCO. The phase detector current is 1 mA.

PRSC_IN (pin 15): RX VCO and TXVCO prescaler input. Usable up to 2 Ghz. The input level should be between -10dBm and 0 dBm. The input impedance will be approximatley 500 ohm // 2 pF plus package parasitics.

5.22 MAGIC / Isolation Amp Interface

The isolation amp is the last receiver stage external to MAGIC. The frequency input to MAGIC will be 215 MHz for both GSM and DCS 1800 with MAGIC Pass 1 and Kramer radio passes 1 to 3. **The frequency input to MAGIC will be 400 MHz for the MAGIC Pass 2 and Modulus radio passes after P3.**

SW_VCC (pin 2): VCC output to the isolation amp. Used to control the isolation amplifier's collector bias. **This line is high during and after the adapt to keep a constant input impedance to the MAGIC preamp input. It toggles low to save current in DRX modes**.

PRE_IN (pin4): IF preamp input. Output of the isolation anmpplifier is impedance matched to the PRE_IN input to MAGIC

6.0 Accessories

6.1 Accessories Supported

Kramer and Leap will support all StarTAC, Krunch, and Zap accessories accept the external headset and DSC to RS-232 data cable used on Krunch/Zap. Kramer / Leap will have an internal boom headset jack and an SCI to RS-232 data cable.
Current Accessories supported:
Fast Charger – StarTAC based AC/DC power supply kit# SYN4278E. This accessory will supply enough power to make a NAMPS or GSM/DCS/PCS call or charge a battery. AC/DC power supply is capable of supplying 1.1Amps continuous or 1.8Amps peak(per GSM requirements). The AC/DC power supply will be recognized via a 33Kohm pulldown on Man_Test to ground. This device will support warm plug.

CLA – StarTAC based Cigarette Lighter Adapter kit# SYN4241A. This accessory will supply enough power to make a NAMPS or GSM/DCS/PCS call or charge a battery. CLA is capable of supplying 1.1Amps continuous or 1.6Amps peak (per GSM requirements). The CLA will be detected via a 33Kohm on Man_Test to ground. Software will not see a difference between a CLA and Fast Charger. This device will support warm plug.

Mid Rate Charger - NAMPS StarTAC based AC/DC adapter Kit# SYN?????. This accessory will supply enough power to charge a battery. Upon detection of the Mid Rate charger (10Kohm on Man_Test) radio will power up into charge only mode. Software will not allow radio to power up into normal operation (camped or keyed). This device will not support warm plug.

Desktop Charger – StarTAC based desktop charger. SCI communication with CHG_En line. Charger will be detected with 33Kohm on Man_Test followed by SCI commands to the desktop charger. This device will support warm plug.

Smart Data Cable – StarTAC based Smart Data Cable is a DSC bus to PCMCIA interface data cable. This data cable is only detected at power up during the DSC bus arbitration. If this data cable is warm plugged in to the radio, the data cable will not be detected until a power cycle occurs. This device will not support warm plug.

Motorola CarKit – SLN3498E is a Motorola designed Digital Handsfree Adapter (DHFA). The DHFA has a internal DC/DC power supply equivalent to a CLA. Upon detection of external power (EXT_B+ interrupt) the radio will detect a 56k pulldown on downlink. The radio will re-synchronize the DSC bus and switch to carkit mode. The internal Echo Cancellor should be on with the Motorola Carkit. This device will support warm plug.
Digianswer CarKit – SYN6348B is a Digianswer designed Digital Handsfree Adapter (DHFA). This DHFA has a internal DC/DC power supply equivalent to a CLA. The Digianswer Carkit also has a DSP for echo cancellation and noise suppression. Upon detection of external power (EXT_B+ interrupt) the radio will detect a 56k pulldown on downlink. The radio will re-synchronize the DSC bus and switch to carkit mode. The Digianswer carkit will have a pull up on Sw_Hook pin# 41 of the peripheral BIC device. This will indicate to software to disable the echo cancellor. This device will support warm plug.

DHFA External Graphics Handset – SCN2636A is a 96x32 graphics External Handset designed to operate with the Motorola or Digianswer DHFA. This device will be detected during the re-synchronization of the DSC bus at power up or during a warm plug. This device has a unique BIC product ID which will be used for identification. This device will support warm plug with a DHFA.

DHFA External 2-Line Handset – SCN????? is a 2-Line character based External Handset designed to operate with the Motorola or Diganswer DHFA and Mobile Transceivers. This device has a unique BIC ID used for identification. This device can be supported but will require software to pre-load prompt differences between 2-Line and Graphic displays. This device will support warm plug with a DHFA.

6.2 Current Accessories not supported:

Zap/Krunch External Headset – SYN6719 will not be supported.

Zap/Krunch DSC to RS232 Data Cable – will not be supported.

Zap/Krunch Wireless Headset – will not be supported.

Analog Audio out the buttplug of Kramer/Leap will not be supported.

6.3 New Accessories supported by Kramer/Leap:

Internal Boom Headset – The radio will have a internal Boom Headset Jack. Insertion of a Headset into the internal Jack will generate a Interrupt (IRQ2). This Interrupt will be exclusive to the Boom Headset. Software will route all DTMF tones and Audio to the headset speaker except for Alert tones. Alert tones will continue to route to the radio alert. At power up the wake up tone should be routed to the headset.

RS232 "Dumb" Data Cable – This data cable will support data calls via the SCI lines out of the buttplug. Hardware will generate a interrupt upon insertion of a data cable. Software will detect this interrupt as IRQ3. After the interrupt is detected software will detect for a 22Kohm pulldown on Downlink and a 22Kohm pulldown on DSC_En. The combination of these two will insure a

"Dumb" data cable is present. DSC_En has to be pulled high by software in any mode regardless of DSC bus state. This data cable will also have flow control (Clear to Send CTS) via WCAP I/O PA4. This device will support warm plug.

6.3.1 Internal Headset support

The Internal Headset will be detected via IRQ2. Upon the falling edge of this interrupt the Internal Headset shall be detected. IRQ2 will be debounced for 480mSec. A low level on IRQ2 will indicate the presence of a headset. Due to having a dedicated interrupt for the headset to A/D measurements are not necessary for the proper detection of the headset. Alert tones will be routed to the radio Alert. All audio and DTMF tones will be routed to the Headset. When the boom headset is present BOOM_EN should be low.

6.3.1.1 DHFA and Headset support

Kramer/Leap will be the first platform to support boom headset with a Digital Hands-Free Adapter. The Headset jack will generate an interrupt when a boom headset jack is inserted. The DHFA will be detected via Ext_B+ and a 56k pulldown on downlink.

If a headset is plugged into the radio and placed in a DHFA the radio will route all Alert tones to the external handsfree speaker.

```
If (External Handset = present) then
    If (Hook state of External Handset = Off Hook) then
            DTMF Tones and Audio routed to Boom Headset Adapter
    Else (External Handset on hook)
            DTMF Tones and Audio routed to Boom Headset Adapter
Else (No External Handset)
    If (Radio Cradle state = Un-Cradled) then
            DTMF Tones and Audio routed to Boom Headset Adapter
    Else (Radio Cradled)
            DTMF Tones and Audio routed to Boom Headset Adapter
```

6.3.2 "Dumb" Data Cable

The Kramer Data Cable is a 3 wire interface (TX, RX, CTS) to the telephone. The data cable uses IRQ3 for detection of the cable. The interrupt will be generated only if a PC is attached.

WCAP PORT	SIGNAL
UTXD	TX Data
URXD	RX Data
URTS_PA5	CTS
IRQ3_PA14	Cable detection

The data cable is powered from the PC and level translators for the data reside in the cable.

CTS is the flow control for the cable. PA5 is used as the control line. A "low" out will alert the PC that the phone is ready to receive data from the peripheral.

The "Dumb" data cable will be detected using an interrupt / A/D measurement scheme. Hardware will generate a interrupt when it detects a 22Kohm or stronger pulldown on Downlink. Hardware will use a 2.85v ±2% voltage detector low current open collector output. Software will use a

negative edge to trigger the interrupt for detection. Software will debounce the line for 480mSec. A low level on IRQ3 will be used by software for presence indication. IRQ3 sould be disabled when a DSC bus accessory is present. Software will go out and take A/D measurements on Downlink and DSC_En.

If (Downlink = 22Kohm) then
    If (DSC_En = 22Kohm) then
        Valid "Dumb" data cable send information on SCI bus.
    Else
        Ignore Krunch Data Cable. No user Interface change.
Else (Krunch Headset)
    Ignore Krunch Headset. No user Interface change or audio routing change.

Software will need to read the A/D state of DSC_En in any mode. Due to this reason software must leave DSC_En high at all times. After software has detected a 22Kohm on Downlink and a 22kohm on DSC_En it will recognize the accessory as a "Dumb" data cable.

6.4 Accessories Matrix

	DHFA (Mot)	DHFA (Digi)	CLA	Kramer Data	Kramer Headset	Desktop Charger	MidRate Charger	Fast Chg
DHFA(Mot)	X	No	No	No	Yes	No	No	No
DHFA(Dig)	No	X	No	No	Yes	No	No	No
CLA	No	No	X	Yes	Yes	No	No	No
Kramer Data	No	No	Yes	X	Yes	No	No	Yes
Kramer Headset	Yes	Yes	Yes	Yes	X	Yes	No	Yes
Desktop Charger	No	No	No	No	Yes	X	Yes	Yes
Mid Rate Charger	No	No	No	No	No	Yes	X	No
Fast Charge	No	No	No	Yes	Yes	Yes	No	X

The matrix above shows all possible combinations of accessories which can be used together.

7. Power Up Sequencing

Upon power up of the phone the following sequence should be used.

GCAP II SPI bits for power up will include:

a) ONOFF1
b) ONOFF2
c) MOBPORTB (low to high transition)
d) Application of power
e) 3SECI
f) PWRON, INT/EXT, and TODA will be ignored

If software sees ONOFF1, ONOFF2, or MOBPORTB bits to be true it will power up the phone. In the case all three of these are false the radio will look at 3SECI. If this interrupt is true the radio will assume a power cut has cause the power up of the phone. In this case the software will jump through a "Soft Reset" to bring the phone up without the end user seeing it. In order for 3SECI to work the PCEN bit must be set at every power up.

If ONOFF1, ONOFF2, MOBPORTB, or 3SECI are not the cause of power up the radio will power back down using WDOG.

7.1 ONOFF Power Up

In the case ONOFF1 or ONOFF2 have caused the radio power up.

a) Verify Ext_B+ is not present, if present go to section 7.2 MOBPORTB Power Up
b) Verify hookswitch state
   -If hs closed and both ONOFF1 and ONOFF2 are active, abort power up sequence and power down.
   -If hs closed, ONOFF2 active, and ONOFF1 inactive, continue power up.
   -If hs open continue power up.
c) DSC_En will be pulled high in hardware, software should not pull DSC_En low
d) Check for Headset, IRQ2 = low, If present wake up tone sent to headset
e) Check for Data Cable, IRQ3 = low, use detection scheme above for data cable
f) Toggle DSC_En in order to force Power On Reset of DSC bus.
g) Use DSC bus arbitration to identify any devices on DSC bus (i.e. EMMI Box, StarTAC PCMCIA Data Cable)

7.2 MOBPORTB Power Up

In the case MOBPORTB has caused the radio power up.

a) DSC_En will be pulled high in hardware, software should not pull DSC_En low
b) Check for Headset, IRQ2 = low, If present wake up tone sent to headset
c) Check for Data Cable, IRQ3 = low, use detection scheme above for data cable
d) Take A/D readings
   1) Man_Test – verify charger and radio cradle state, use Man_Test spreadsheet attached
   2) Downlink – check for accessory type, DHFA or Data Cable, use Downlink spreadsheet attached
   3) Uplink – No A/D measurements needed.
   4) DSC_EN – verify "Dumb" data cable and ignition state, use DSC_En spreadsheet attached
e) If "Dumb" data cable is not attached and charger is present (Midrate or Fast Charger) send SCI command to Desktop Charger every ??sec for presence detect.
f) Toggle DSC_En in order to force Power On Reset of DSC bus.
h) Use DSC bus arbitration to identify any devices on DSC bus (i.e. DHFA, Handset, EMMI Box, StarTAC PCMCIA Data Cable)

7.3 3SECI Power Up

In the case a power cut has caused the radio power up.

a) If a power cut is found to be the reason of power up 3SECI=True
b) Go into software reset loop if 3SECI = true
c) Check RAM for valid SIM Pin.

d) If MOBPORTB=true use section 7.2
e) Else use section 4.1 for power up
f) No wake up tone or wake up graphics shown

1. Power Down Sequencing

Upon power down the following sequence should be used.

Following is a list of possible power down causes.

1) ONOFF1 or ONOFF2
2) Low B+ voltage
3) Software power down – Factory bit set
4) Power Cut / Hardware power down

1) ONOFF1 or ONOFF2

ONOFF1 will be tied to the internal power key of the radio. ONOFF2 will be tied to Audio_Out/ONOFF of the external connector (Buttplug) and the internal power key.

Radio flip open – if either ONOFF lines cause a interrupt the radio will power down.

Radio flip closed – if ONOFF1 and ONOFF2 generate an interrupt ignore it. If ONOFF2 alone generates an interrupt the radio will power down.

Kramer Interface Sign Off

Name	Position	Signature
Ross Ripley	Hardware Manager	
Joe Hansen	Software Manager	

DUALBAND KRAMER

HEAD_INT
(Keyboard) KBR0, KBR1, KBR2
KBC0, KBC1, KBC2, KBC3
BKLT_EN
DP_EN
HS_INT
VIB_EN
LED_RED
LED_GRN
LS1_IN
LS2_IN
LS3_TX
LS3_RX
CLK_SELCT
TX_EN
DM_CS
TX_KEY
RX_EN
RX_ACQ
RESET
(SDTX) BDX
(TX_CLK) BCLKX
from / to MAGIC
(SCLK_OUT) BCLKR
(SDFS) BFSR
(SDRX) BDR

15 PIN EXT CONN. J 600

DSC_EN 13
RS232_RX 7
RS232_TX 6
BATT_FDBK 4
SW_RF 2
EXT_CHG_EN 8
EXT_B+ 14
GND 1
GND 3
GND 10
GND 15
MAN_TEST_AD 5
ON / OFF 9
UPLINK 11
DOWNLINK 12

VR830
EXT_B+

U700 WHITE_CAP

KEYPAD DISPLAY INTERFACE
SIM INTER FACE
CTM MODULE
SERIAL INTER FACE
DSP
DSC
UART INTERF.
SPI INTERFACE
CPU
MEMORY INTERFACE
CTM
A / D
SPI INTERFACE
TIMER

C14, D4, E12, H4, J10, K6, N12
B5, B9, B10, G12, K14, L11, N8
(CE) MQSPI_CS1
(SPI_CLK) MOSPI_CLK1
(SPI_DATA) DX1
(MAGIC SPI)
V2
V3

DATA BUS
ADDRESS BUS

(Flip Con.) R_W
CE2
CE3
R_W
U702 SRAM
D6, E1
B2
A1
G6

V2
RESET
CE0
CE1
U701 EPROM EEPROM
A4, A6, F6
B4
D7
F8

J700 FLIP CON.
D7 - D0
7, 9, 10, 11, 13, 14, 15, 17
A0
19
V2
RESET
R_W
DP_EN
BKLT+
GND
RTC_BATT
3, 4, 6, 12, 16
22
18
21
1
2, 6 ,24, 26
27

-5V_EN
LS_V1
U901
-5V
STDBY
LS_V1
DEEP SLEEP CIRCUIT
V1

BATT_PD
BATT_SER_DATA
CHRGC
ISENSE
BATT CON. J604
GND
V2
BATT_PD
EXT_B+
R932
Q932
BATT+ 1, 2, 5, 6
THERM
U950
B+
Q942
1, 2, 3
CR940
BATT_THERM
CHRGC
ISENSE
BATT+
EXT_B+
CLK
PD
SIM_I/O
LS1_IN
LS2_IN
LS3_TX
LS3_RX
PWR_SW
STDBY
RESET

(WhiteCap) HS_INT
KBR0, KBR1, KBR2
(WhiteCap)
KBC0, KBC1, KBC2,KBC3
(GCAP2) PWR_SW
(Q938) BKLT+
(GCAP2) V2
KEYBOARD

(WhiteCap) VIB_EN
B+
U801
J810 J811 VIBRA CON.
(GCAP2) V2
LED_RED
(WhiteCap)
LED_GRN
Q805
Q805

AUDIO SPI
GCAP SPI
GCAP_CLK 13 MHz
GCLK 32.768 KHz
MAGIC_13MHz
RTC_BATT
Y900

U900 G_CAP2

SPI INTERFACE
REAL TIME CLOCK
CHARGE SELECT SENSE
LEVEL SHIFT
SENSE CNTL.
Logic Control
Interface Audio Codec
PA_DRV
VREF REG.
V3 REG.
V2 REG.
V1 REG.
VSIM REG.
VBOOST1 REG.

DSC_EN_AD
DOWNLINL_AD
BATT_THERM
ISENSE

J900 SIM Con.
VSIM1

VREF 2.775V,for GCAP
V3 1,8V, for WhiteCap
V2 2.775V, for WhiteCap logic outputs, RAM, FLASH, EEPROM
LS_V1 5.0V, for DSC Bus, Negative Voltage Regulator
VSIM1 3.0 or 5.0V, for SIM Card Circuit

MIC
U980
J650
HEADSET CON.
V2
HEAD_INT

SPKR
ALRT
SPR-
SPR+
ALRTOUT
ALRT_VCC

Q938
L901
CR901
V_BOOST1 Internal GCap use only (VSIM1, LS_V1)
B+
BKLT_EN
Q939
BKLT+ (Flip Con.)

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RX SIGNAL PATH
TX SIGNAL PATH
MAIN VCO SIGNAL PATH
TUNING VOLTAGES
REFERENCE CLOCK
Orderable Part
Non - Orderable Part

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LEVEL 3 AL Block Diagram	Rev. 1.5
Dualband Kramer	
Ralf Lorenzen, Michael Hansen, Colin Jack, Ray Collins	Page1

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DUALBAND KRAMER

A1

GSM_LNA275
DCS_LNA275
EXT ANT
SW_RF
U101
SWITCH CONTROL CIRCUIT
MIX_275
PAC_275

GSM_LNA275
GSM LNA
FL460
925-960MHz
Q461
FL470
925-960MHz
MIX_275
1805-1880MHz
FL450
Q451
1805-1880MHz
FL465
DCS_LNA275
MIX_275
Q1254
Q1254

EGSM: 880-915Mhz
DCS: 1710-1785MHz
B+
1-3
U341
4
DM_CS
5
PA_B+
FL300
U300 DCS PA
U400 GSM PA
CR300
CR301
Q300
Q400
Q455
CR306,307
GSM_PINDIODE
-5V
SHIFT LEVEL CIRCUIT
PAC_275
U340 PAC
DET
SAT.
RF_IN
PAC_275
4, 14
1, 3
NPA_MUTE
U341
PA_B+

EGSM: 880-915Mhz
DCS: 1710-1785MHz

EGSM: 1325-1360MHz
DCS: 1405-1480MHz
RVCO_250
RX VCO
DCS_VCO
CR251
CR250
C257
Q262
Q253
Q255
U250
TX VCO
TX LOOP FILTER
SF_OUT
Q344
Q343
TX_EN
TVCO_250
(GSM / DCS SELECT)
RVCO_250
(RX VCO, GSM/DCS SELECT)
PAC_275
G_TX_VCO
D_TX_VCO

RX LOCAL OSCILLATOR
Osc. discrete circuty Q1255
800MHz
CR259
V1
FL457
400 MHz
Q490
SW_VCC
RF_V2
Q242
B+
RF_V1
Q240

U913 MAGIC
PLL
STEP ATT.
DEMODULATION
RXI
RXQ
RX SPI
(SCLK_OUT) BCLKR
(SDFS) BFSR
(SDRX) BDR
to WhiteCap
SWITCH
REG.
VRef
PHASE DET
Divider 200KHz
13MHz
CR230
SWITCH
SUPER FILTER
MUX
MAGIC_13MHz
to WhiteCap
CLK_SELCT
from WhiteCap
Startup Ref.
1 / 2
SF_OUT
PHASE DET
Divider
PLL
AFC
Prog. Divider 200KHz REF.
REF. OSC. 26 MHz
26MHz
Y230
V1
DCS_SEL
LOGIC CONTROL
SPI INTER FACE
(CE) MQSPI_CS1
(SPI_CLK) MOSPI_CLK1
(SPI_DATA) DX1
from WhiteCap
GP04
MODULATION
TXI
TXQ
TX SPI
(SDTX) BDX
(TX_CLK) BCLKX
DETECT_SW
AOC_DRIVE
SAT_DETECT
TX_KEY_OUT
PA CONTROL
LOGIC CONTROL
RX_ACQ
DM_CS
TX_KEY
from WhiteCap

NPA_MUTE
TVCO_250
PAC_275
DCS_VCO
MIX_275
GSM_LNA275
DCS_LNA275
G_TX_VCO
D_TX_VCO
GSM_PINDIODE

GSM / DCS SELECT CIRCUIT

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Dualband Kramer	
Ralf Lorenzen, Michael Hansen, Colin Jack, Ray Collins	Page1

RX SIGNAL PATH
TX SIGNAL PATH
MAIN VCO SIGNAL PATH
TUNING VOLTAGES
REFERENCE CLOCK
Orderable Part
Non - Orderable Part

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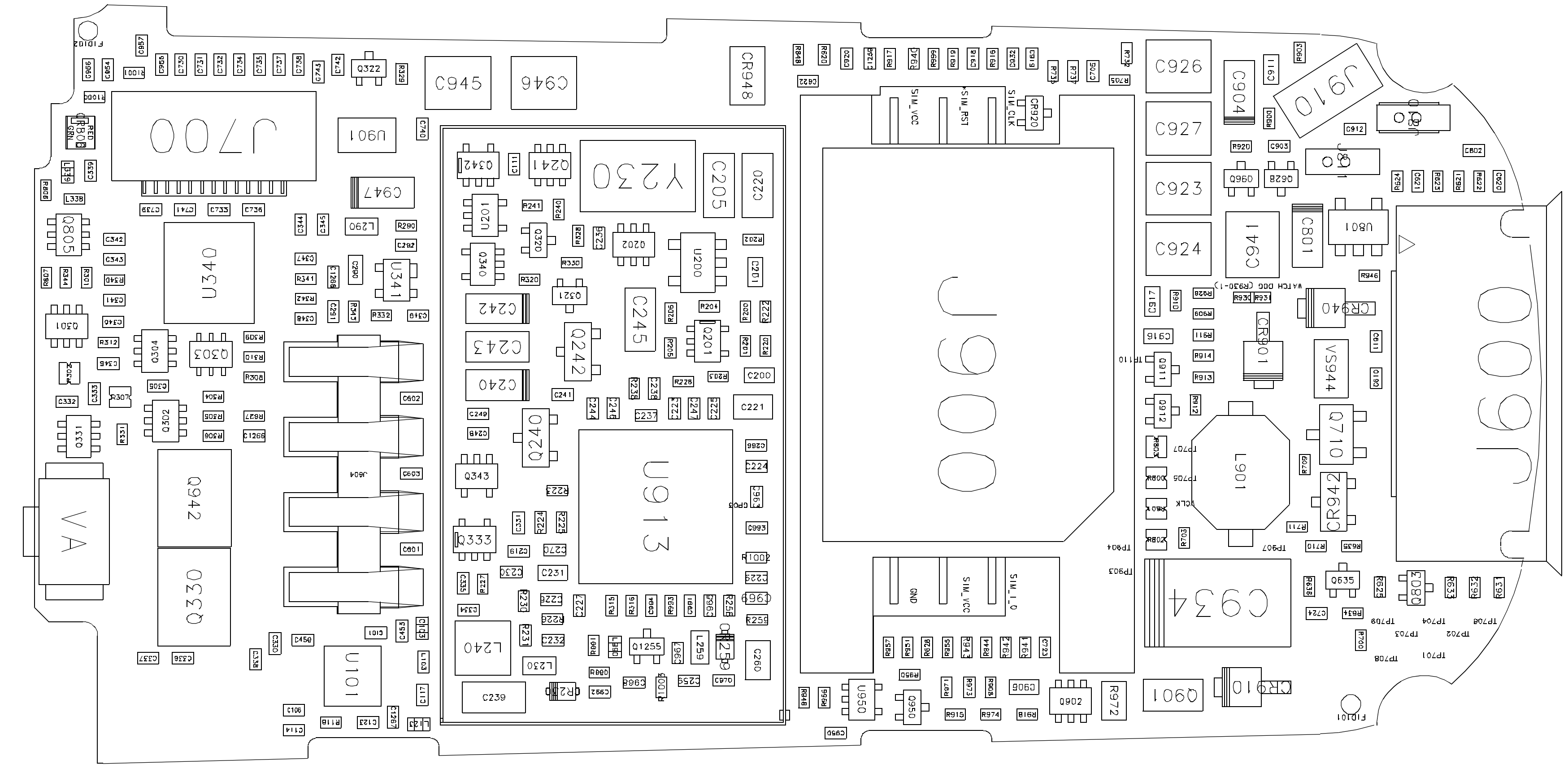
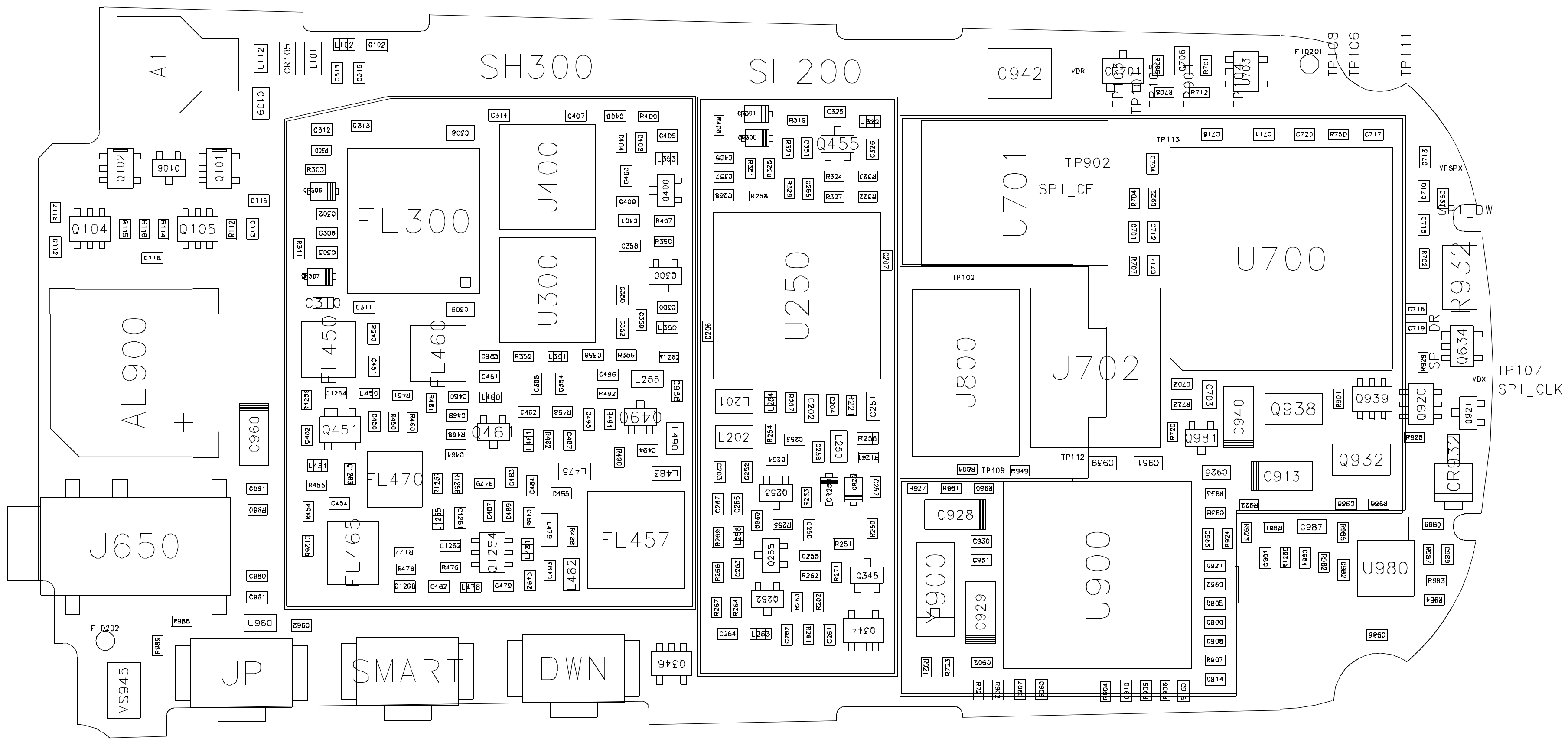
Dual Band KRAMER H13





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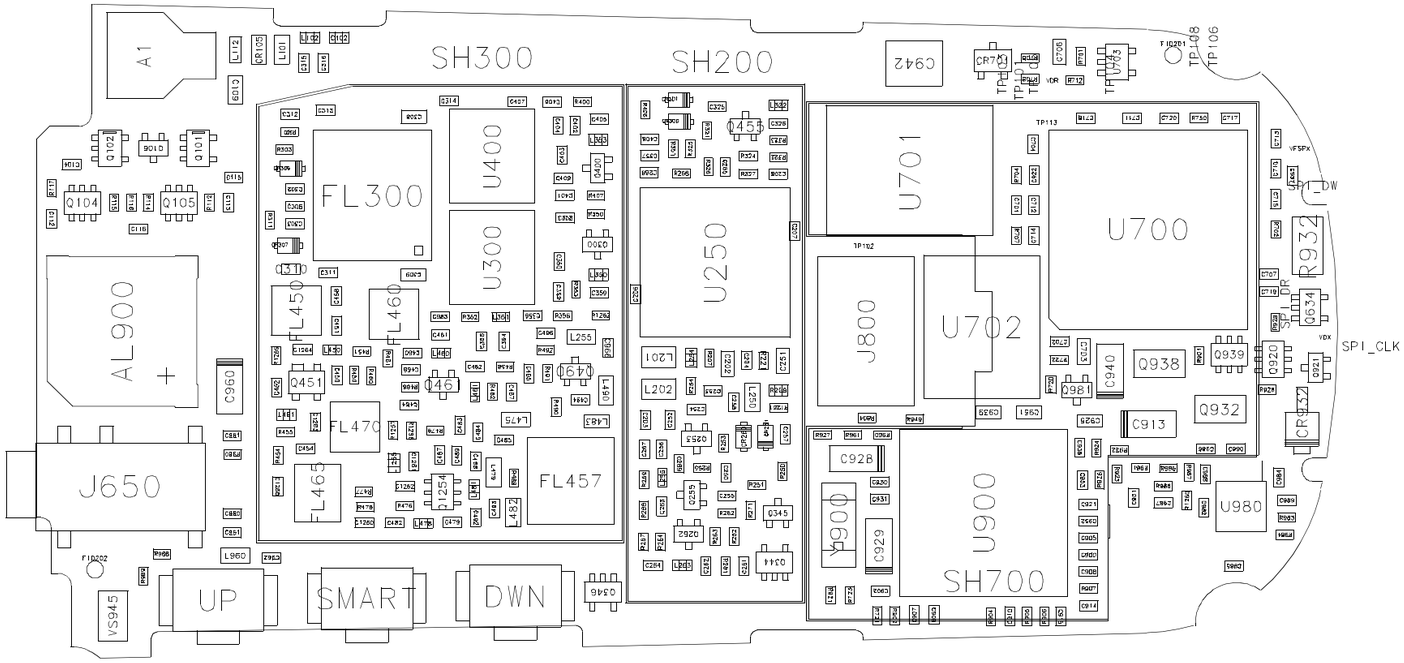
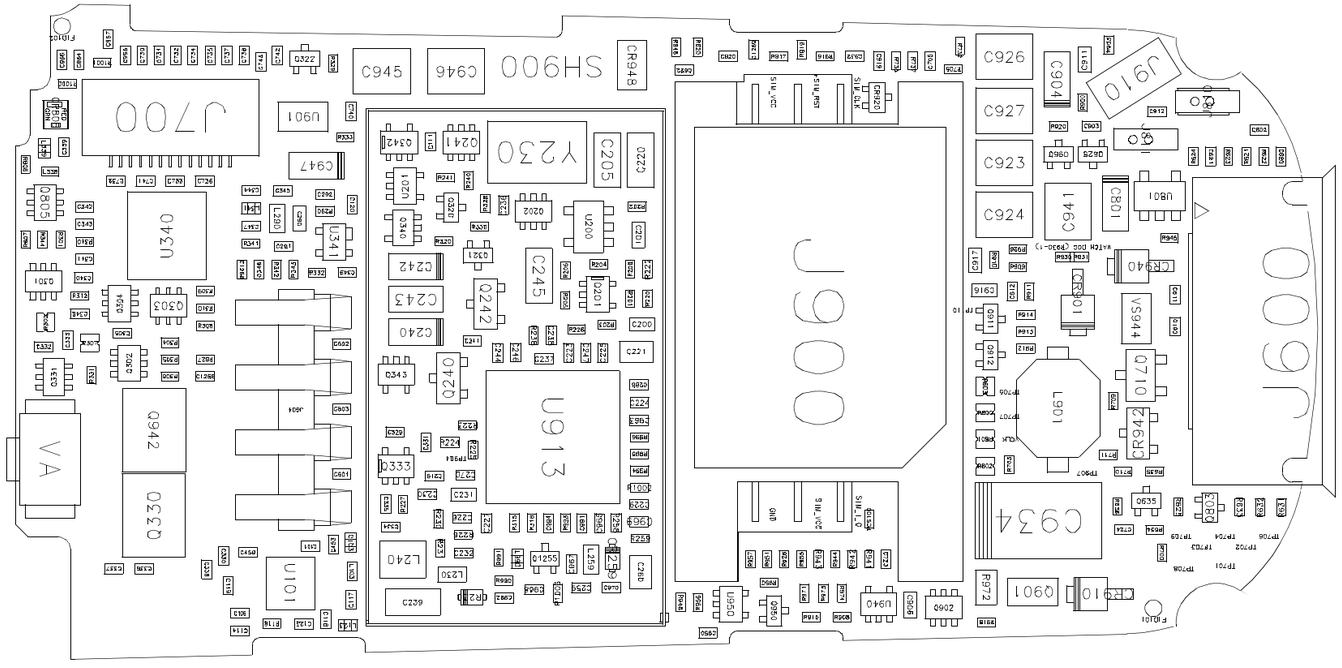
DUALBAND KRAMER H23





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LEVEL 3 LAYOUT	Rev. 1.0
DUALBAND KRAMER H23	
Ray Collins, Ralf Lorenzen, Michael Hansen	Page1

Dual Band KRAMER P11

GSM KRAMER TRANSCEIVER
P/N 84M0057M1
SHEET 2 OF 3

ISS.	COMMENTS	DATE
P1_v1	COPIED FROM M+M0057M1	06/03/97
P1	RF RELEASE	10/28/97
P1_.2B	P1 RELEASE	11/25/97
P2_.3A	RELEASED FOR PROTOTYPE	02/03/98
P3_.v2	RELEASED FOR PROTOTYPE	04/06/98
P4_.v2	RELEASED FOR PROTOTYPE	06/25/98
P4.1_.v3	RELEASED FOR PROTOTYPE	06/30/98
P4.2b_.v1	VALUE CHANGES	07/14/98
P4.3_.v3	VALUE CHANGES	07/15/98
P4.2	RELEASED FOR PROTOTYPE	07/22/98
P4.3	RELEASED FOR PROTOTYPE	07/28/98
P5	RELEASED FOR PROTOTYPE	08/12/98
P5.1	RELEASED FOR PROTOTYPE	08/28/98
P5.2	RELEASED FOR PROTOTYPE	09/04/98
P6	RELEASED FOR PROTOTYPE	09/21/98
P7	RELEASED FOR PROTOTYPE	10/05/98
P7.1	RELEASED FOR PROTOTYPE	10/12/98
P7.2	RELEASED FOR PROTOTYPE	10/19/98
P7.3	RELEASED FOR PROTOTYPE	10/26/98
P8	RELEASED FOR PROTOTYPE	10/30/98
P9	RELEASED FOR PROTOTYPE	11/02/98
P10	RELEASED FOR PROTOTYPE	11/04/98
P11	RELEASED FOR PROTOTYPE	11/06/98

Ref #'s 450-469

GSM_LNA275 MIX_275

FL460 942.5MHz 31-E0945X302

Q461 NE68715 48-09527E30

GSM LNA

FL470 942.5MHz 31-E0945X302

Ref #'s 470-489

MIXER

L479, L482 SHOULD BE 24-09350L SERIES

GSM_LNA275 MIX_275

Q1254

DCS_LNA275

FL457 400MHz 31-E0787X01

Ref #'s 490-500

ISO. AMP

Q490 NE68719 48-09527E30

RX MID CHANNELS
GSM: CH 62 -- 947,4 MHz
EGSM: CH 37 -- 942,4Mhz
DCS: CH 700 -- 1842,8MHz

DCS LNA

DCS_LNA275 MIX_275

FL450 1805-1880MHz 31-E0815E01

Q451 BFG520

FL465 1842,5MHz 31-E0785X01

RF SWITCH

Ref #'s 100-150

A1 31-E0374X01

U101 GC7130

DCS_LNA275 GSM_LNA275 PAC_275 MIX_275

Q101 BFG520L

Q102 BFG425W

Q105 BFG520L

Q106 BFG425W

Q104 BFG425W

-5V_SW -5V

SW_RX

RX VCO

RX VCO MID CHANNELS
GSM: CH 62 -- 1347,4 MHz
EGSM: CH 37 -- 1342,4Mhz
DCS: CH 700 -- 1442,8MHz

RX VCO FRQ. RANGE
EGSM: 1325 - 1360Mhz
DCS: 1405 - 1480MHz

RVCO_250 SF_OUT DCS_VCO

Q262 BFG520W/X

Q255 BFG520L

Q253 BFG520W/X

CR250 CR251

NOTE: All other connections are ground.

RF_V2 RF_V1

Q1255 NE68719

CR259 BB909

BCLKR 13MHz CR230 BB833

U913 MAGIC_IC DL-MAGIC

MAGIC

BCLKX CLK_SELECT TX_KEY BSM_CS MQSPI_CS1 MQSPI_CLK1 DX_1 DDX SPI BUS

MAGIC_13MHz

Q225 BFG425W

Q240 BFG425W

Q242 BFG425W

Y230 26MHz 48-09553J02

Vref

Q241 BFG425W

V1_FILT

TX_KEY_PAC DET_SW SAT_DET

Q343 MP_B_MMIC UMC5

Q344 MP_B_MMIC UMC5

48-E0933G05

(WhiteCap) TX_EN

(Magic) SF_OUT

(Q333) TVCO_250

(RX VCO, Q345) RVCO_250

(Magic) RF_V2 (RX LNA, Mixer) MIX_275 Q340 BFG425W

48-E0933G05

RX_EN (WhiteCap)

(GCap) V1_FILT (Magic) V1_SW Q346 BFG425W

TX_EN (WhiteCap)

GSM-DCS SELECT

RVCO_250 (Q344) MIX_275 (Q340) TVCO_250 (Q343)

GSM_LNA275 (RX LNA, MIXER) DCS_LNA275

(RX VCO) DCS_VCO

(TX VCO, TX EXITER) D_TX_VCO G_TX_VCO

Q342 BFG425W

Q345 BFG425W

U201 UPG4157TB

Q333 UPG4157TB

48-E0933G07

DCS_SEL GSM_SEL

TX VCO FRQ. RANGE
EGSM: 880-915Mhz
DCS: 1710-1785MHz

TX VCO MID CHANNELS
GSM: CH 62 -- 902,4MHz
EGSM: CH 37 -- 897,4Mhz
DCS: CH 700 -- 1747,8MHz

TX_VCO

D_TX_VCO G_TX_VCO SF_OUT

U250 1747,5MHz 897,5MHz

PAC_275

TX_EXITER

PAC_275

CR300 CR301

Q455 BFG425W/X

LOOP FILTER

U200 NOTE: Q201, Q200 ARE DNP'd

Q201 BFG425W

Q202 BFG425W

V1_FILT

DM_CS TX_EN

SAT_DET DET_SW TX_KEY_PAC

PA_B+ VCTRL PAC_275

Q330 BFG425W

Q331 BFG425W

DM_CS Q331

U300 SKY77318

Q300 BFG425W

FL300 900/1800MHz

TX FRQ. RANGE
EGSM: 880-915Mhz
DCS: 1710-1785MHz

U400 SKY77318

Q400 BFG425W

GSM_PINDIODE CR306 BAR64-02W

GSM_PINDIODE CR307 BAR64-02W

Q303 BFG425W

Q304 BFG425W

Q302 BFG425W

Q301 BFG425W

-5V_SW D_TX_VCO VCTRL G_TX_VCO

U340 SC-70-6-6GTB

U341 NC7SZ07

NPA_MUTE PA_B+

P.A. CONTROL

F11 IS ACTUAL CORRECT PART

GSM Service Support
Level 3 Authorized

REVISIONS

GSM SERVICE SUPPORT GROUP	01.10.99
LEVEL 3 COLOUR SCHEMATICS	Rev. 1.2
GSM KRAMER RF	
Ralf Lorenzen, Ray Collins, Michael Hansen	Page 2of 3

Europe, Middle East & Africa
Customer Services
Level 4 Authorised

Kramer

Dual Band
GSM CELLULAR PHONE

Global Customer Services Policy

Issue 1.0
15th Dec 1998

Motorola Inc.
Cellular Subscriber Sector
European Cellular Subscriber Group
Easter Inch, Bathgate
West Lothian EH48 2EH, Scotland

PURPOSE

This document specifies the Customer Service requirements to provide after sales support for the Kramer Product Series.

CONTENT

SECTION 1.0 - SERVICE POLICY

1.1 Warranty:

Product will be sold with the standard 12 months warranty terms and conditions. Accidental damage misuse, retailers extended warranties will not be supported under warranty. Non warranty repairs will be available at agreed fixed repair prices. Proof of purchase will be required to validate warranty claims.

1.2 Out Of Box Failure Policy:

The standard OOB Failure criteria will apply. Early life customer units which fail within less than 30 minutes as measured by the Life Time Call Timer, to be returned to Manufacturing for root cause analysis, to guard against epidemic criteria. Manufacturing to bear the costs of early life failure.

1.3 Product Support:

Customer's original telephones will be repaired but not refurbished as standard.

The first 100 consecutive failed products returned to Motorola will be returned for root cause analysis directly to the core engineering group in Libertyville. These fails will include both out of box and field failures, and units sent should include all accessories. These shipments will be co-ordinated through the service support team.

The next 200 consecutive failures will be returned directly to the nearest Motorola Hi-tech centre for root cause analysis. The results of this analysis will be fed back to the core engineering group. The results of both exercises will be documented and distributed in procedure format to all relevant repair points.

When new manufacturing sites are brought on-line, after prime site ship acceptance, the first 200 consecutive field failures from that factory will be returned to the nearest hi-tech centre for root cause analysis. The data generated from this exercise will be fed back to the site of manufacturing and the results will be documented and distributed in procedure format.

The initial 300 returns will be swapped for complete kits, and all returned units must be accompanied by their respective accessories pack. The country customer service manager is responsible for ensuring that the necessary materials are available upon customer demand.

For the first 3 to 6 months in the field, only Motorola Hi-Tech Centres will perform all repairs in order to give accurate and detailed feedback to engineering. Only limited component repairs can be carried out on Kramer due to the new board technology used. If the suspected faulty component cannot be safely replaced using a soldering iron, then the relevant assembly should be scrapped. No heat gun or BGA Repair Tool should be used on Kramer due to the type of PCB used and the bonding agent used on some BGA components.

In some instances further samples will be required by engineering for analysis either by the core team or the hi-tech centre.

1.4 Customer Support:

Customer support (End user) will be available through dedicated Call Centres and In Country Help desks.

SECTION 2.0 - SERVICE REQUIREMENTS

2.1 Training and Documentation

Level 1 Service will be replace for new & Level 2 Service will include the repair of main mechanical parts only.

Documentation Available:

* User Manual
* Accessories Manual
* Level 1 and 2 Service Manual
* Level 1 and 2 Parts List

Training:

Training will be carried out if necessary, by local training representative.

Level 3 Service will consist of repair of all main mechanical parts and also top 30-40 electrical parts, by external Motorola Authorised Repair Centres only.

Documentation Available:

* Level 3 Block Diagrams and Signal Flows
* Repair Flow Chart
* Training Slides
* Level 3 Limited Parts List
* Full Board Overlays

Training

Level 4 training will be given to all Regional Technical Trainers who will in turn provide training for all Level 3 hubs in their regions.

Level 4 Service will consist of repair of all fails including those not repairable by Level 3 Centres. This will be done in Motorola Hi-Tech Centres only.

Documentation Available:

* Full Schematics
* Product Description
* Interface Document
* Level 4 full parts list

Training

Level 4 training will be given to all hi-tech analysers due to be working on the product in its initial 6 months in the field.

2.2 Test Equipment and Tools:

Service Tools, test equipment and software updates will be recommended for Level 1, 2, 3 and 4 Servicing.

SECTION 3.0 -QUALITY REPORTING, METRICS

3.1 Field Return Rate:

The 1998 Projected Field Return Rates = TBA (Based on Engineering ALT Results)

3.2 Field product performance to be monitored using EPPRS system.

Monthly repair data can then be provided to Engineering which includes:
* % field return rate,
* paynter chart (failure by month of manufacture)
* Repair Analysis
* Component Analysis (Top 10 Component failures)

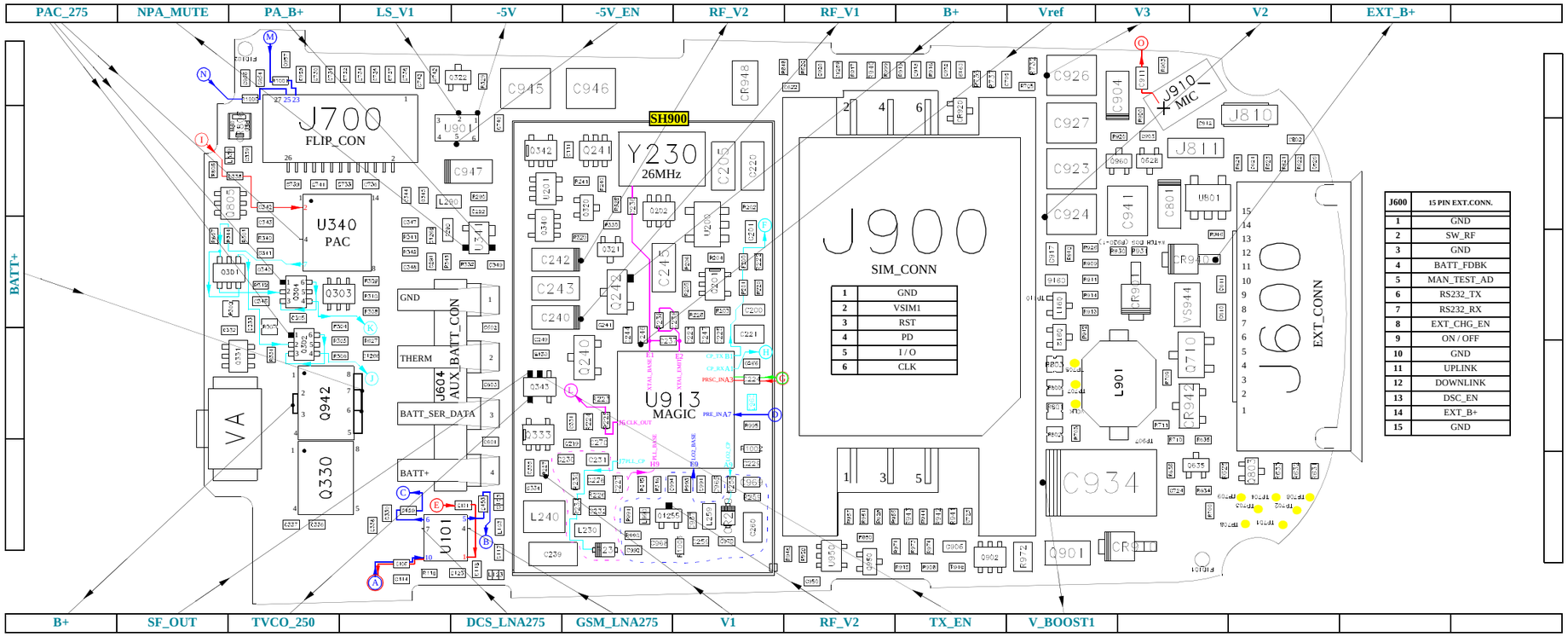
3.3 Field Returns Improvement Plan:

68% year on year (Q4-Q4) reduction in the Service Bounce Rate.

Europe, Middle East & Africa Customer Services

Level 3 Authorised

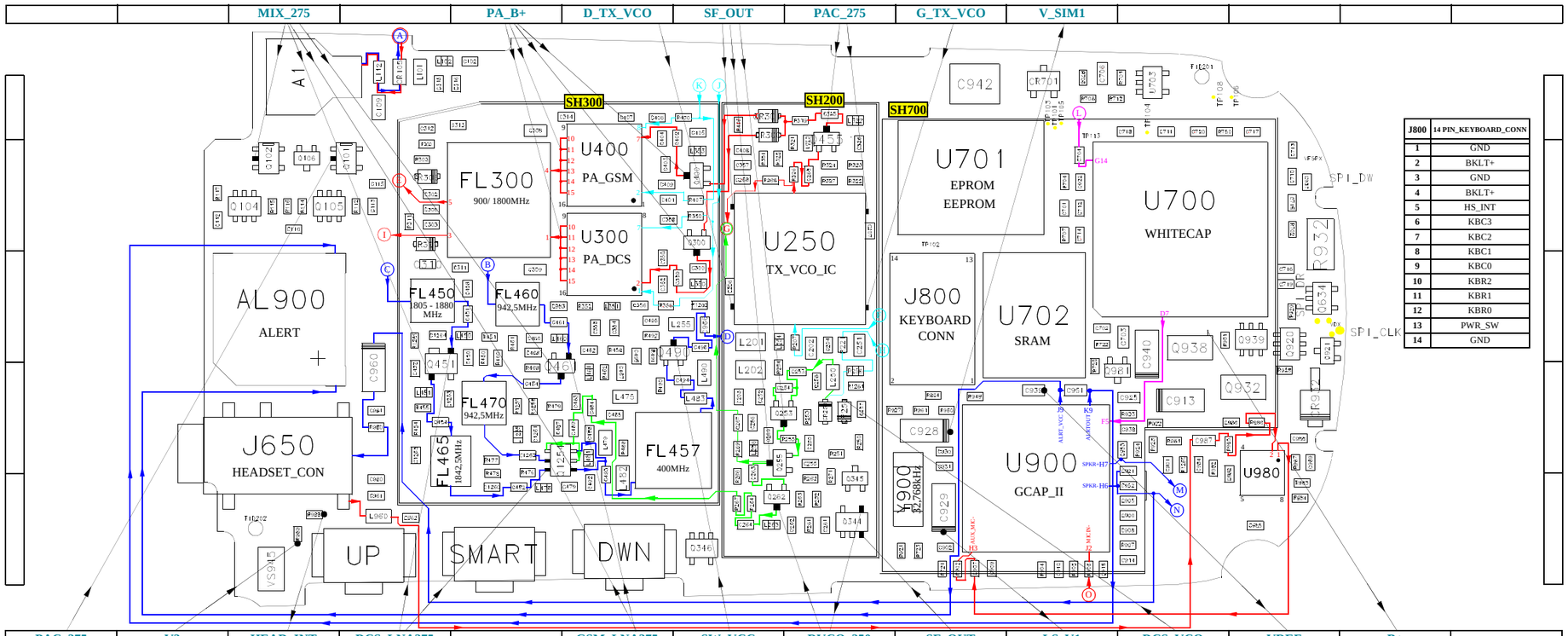
Dual Band KRAMER H13



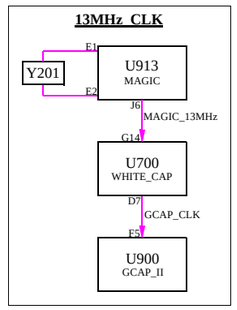
J600	15 PIN EXT.CONN.
1	GND
2	SW_RF
3	GND
4	BATT_FDBK
5	MAN_TEST_AD
6	RS232_TX
7	RS232_RX
8	EXT_CHG_EN
9	ON / OFF
10	GND
11	UPLINK
12	DOWNLINK
13	DSC_EN
14	EXT_B+
15	GND

J600	27_PIN_FLIP_CONN.
1	BKLT+
2	GND
3	V2
4	V2
5	V2
6	GND
7	D7
8	NC
9	D6
10	D5
11	D4
12	V2
13	D3
14	D2
15	D1
16	V2
17	D0
18	R_W
19	A0
20	NC
21	DP_EN
22	RESET
23	SPKR+
24	GND
25	SPKR-
26	GND
27	RTC_BATT

A	RX / TX ANTENNA SIGNAL
B	GSM RX ANTENNA SIGNAL
C	DCS RX ANTENNA SIGNAL
D	AMPLIFIED RX ANTENNA SIGNAL
E	FILTERED PA OUTPUT SIGNAL
F	TX VCO TUNING VOLTAGE
G	TX / RX VCO FEEDBACK LINE TO MAGIC
H	RX VCO TUNING VOLTAGE
I	PA DETECT LINE
J	PA TUNING VOLTAGE
K	PA TUNING VOLTAGE
L	MAGIC 13MHz
M	RX SPEAKER LINE+
N	RX SPEAKER LINE-
O	TX MIC LINE+



J800	14 PIN_KEYBOARD_CONN
1	GND
2	BKLT+
3	GND
4	BKLT+
5	HS_INT
6	KBC3
7	KBC2
8	KBC1
9	KBC0
10	KBR2
11	KBR1
12	KBR0
13	PWR_SW
14	GND



TP	
101	R_W
102	CE_0 Eprom
103	CE_1 Eprom
104	CE_3 SRam
105	CE_2 SRam
701	Earth
702	TMS
703	TD0
704	TRST*
705	EMU_1
706	TD1
707	EMU_0

EUROPE MIDDLE EAST & AFRICA CUSTOMER SERVICES	04.02.99
LEVEL 3 COLOUR SIGNAL FLOW	Rev. 1.0
Dual Band Kramer	
Ray Collins, Ralf Lorenzen, Michael Hansen, Colin Jack	Page1

MOTOROLA

series™

DUAL-BAND MOBILE TELEPHONE

V.small V.light V.desirable ...
and now V.colours

Model V.3688

GSM 900/1800 MHz

MOTOROLA

series™

DUAL-BAND MOBILE TELEPHONE

Introducing the Motorola V.3688 in two new colours

Model V.3688

GSM 900/1800 MHz

MOTOROLA

series™

DUAL-BAND MOBILE TELEPHONE

Express Yourself

- **Now exists in three distinctive and unique colours:**
  - Black
  - Radar Blue
  - Titanium

- **1999 Motorola Quantitative Research showed the new colours to be:**
  - Classy
  - Smart
  - Bright
  - Eye-catching
  - Modern

Model V.3688
GSM 900/1800 MHz

MOTOROLA

V. series™

DUAL-BAND MOBILE TELEPHONE

The Story So Far

- V. series launched in March 1999 in EMEA as the smallest and lightest GSM Dual-band phone in the world
- Black colour well received by consumers
- Launched with heavyweight pan-EMEA advertising
- Supported by dedicated PR and promotional material
- Distributed in all mainstream outlets

Model V.3688
GSM 900/1800 MHz

MOTOROLA

series™

DUAL-BAND MOBILE TELEPHONE

The Brand Promise

- **Show your world that you've made it**

Model V.3688
GSM 900/1800 MHz

MOTOROLA

V. series™

DUAL-BAND MOBILE TELEPHONE

The Brand Character

- Stylish
- Outgoing
- Trend-setting

Model V.3688
GSM 900/1800 MHz

MOTOROLA

V. series™

DUAL-BAND MOBILE TELEPHONE

Target Consumer

- Those who seek products that will help them feel important within their group
- Those who like to have fun by keeping in touch with their friends
- These consumers choose products with badge value to convey an image of success
- Men and women between the ages of 18-34
- Those who are more willing to pay for products they value
- They like to be noticed using a distinctive communications device

Model V.3688
GSM 900/1800 MHz

MOTOROLA

series™

DUAL-BAND MOBILE TELEPHONE

Key Benefits

- **Functional**
  - **One of the smallest and lightest phones in the world**
  - **Ease of use, portability**
  - **External badge**
- **Emotional**
  - **“Look at Me”: Tells everyone that I have style**
  - **Colour for colourful me**
  - **I’m modern, elegant, youthful and fun**
  - **Self fulfilment and self expression**

Model V.3688
GSM 900/1800 MHz

MOTOROLA

V. series™

DUAL-BAND MOBILE TELEPHONE

Product Features

- Amazingly small and colourful
- SMS (Short Message Service) capable
- VibraCall™ alert
- Optimax™ full graphics
- Hands-free headset accessory
- New mini Rae charger
- Increased talktime and standby time due to new 600 mAh Lilon battery as standard

Model V.3688
GSM 900/1800 MHz

MOTOROLA

series™

DUAL-BAND MOBILE TELEPHONE

Quick Reference Guide

Basic Operation

Turn phone on/off	Press ⏻
Place a call	Enter phone number and press OK
Receive a call	Open phone or press OK, 4✱ or #▶
End Call	Close phone or press OK, C
Quick Access	Press ↑ to enter Quick Access menu
Access Options & Phone Book Menu	Press MENU
Select entries & menu options	Press 4✱, #▶
Accept call, setting, option	Press OK
Reject call, setting, option	Press C
Add phone book entry	Press M+
Call Voicemail	Press 1.

Quick Access Interface

To enter	Press ↑
To scroll functions	Press 4✱, #▶
To select function	Press OK
To directly select a function	Press ↑ and any number (1 – 9), then press OK.

Store to Phone book

Name and number	Press M+. Press OK to select phone memory or 4✱, OK to select SIM card memory. Enter phone number. Press OK. Enter name, using letters on key 0 – 9, #▶ to advance, 4✱ to back space. Press OK. Enter location number. Press OK.

MOTOROLA

series™

DUAL-BAND MOBILE TELEPHONE

Quick Reference Guide

Memory Dialling

Recall by name	Press Smart Button, use side keys to scroll to name or press first letter of the name
Last 10 Numbers Dialled	Press OK, then scroll through Last Ten Calls. Press OK to call the number.

MOTOROLA

V. series™

DUAL-BAND MOBILE TELEPHONE

Quick Reference Guide
Special Features

Control

- **Customisable Quick Access Menu**
  - Place nine of your most frequently used features in your own personal menu so that they can be accessed with just two key presses. Icons make each feature easy to identify.

Power

- **Superb battery performance**
  Each phone is capable of several hours conversation or several days standby, but is still small and light. Use both 900 and 1800 MHz bands for greater call success and allow wider roaming opportunities.

Model V.3688
GSM 900/1800 MHz

MOTOROLA

series™

DUAL-BAND MOBILE TELEPHONE

Quick Reference Guide
Special Features

Discretion

- **VibraCall™**  **- In locations where you don't want your phone to ring, or which are too noisy to hear your phone ring, your phone can vibrate to alert you of a call.**

- **Wearable Holster - Wear your phone in a stylish holster on your belt. It is small enough and light enough to keep with you almost anyway.**
- **Stop Call Alert - Press either volume buttons when the phone is ringing or vibrating. This will stop the alert but not answer the phone.**

Model V.3688
GSM 900/1800 MHz

MOTOROLA

series™

DUAL-BAND MOBILE TELEPHONE

Quick Reference Guide
Special Features

Personality™

- **Unique to Motorola. Personality ™ allows you to personalise the way you use your phone - for example, different ringer tones, a phone book and network selection preferences - all presented with clarity and simplicity, identifiable with an OK symbol.**

Model V.3688
GSM 900/1800 MHz

MOTOROLA

V series™

DUAL-BAND MOBILE TELEPHONE

Accessories

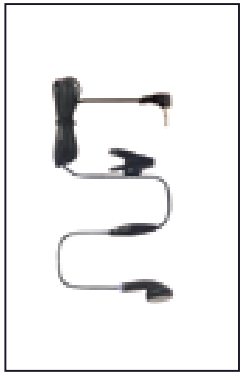
Carry Solutions

Smart Leather Case
Black CCA9060
Tan CCA9061

Leather Pouch
Black CCA9050
Tan CCA9051

Plastic Holster
CCA9150

Hands-free Accessories



Portable Hands-free Kit
HSK9000

In-car Accessories

In-car Phone Charger
CLA9000

Chargers

Mini Travel Charger with Euro Plug
CHA9050
With UK Plug
CHA9060
Mini Desktop Charger Base
CHA9250

Car Kits

Professional DSP VR Hands-free Car Kit
HFK9450A

Smart Handset

Smart Handset for DSP Car Kit
HSK9380

Data Solutions

Smart CELLect™
PCC9050
56k Global Modem PC Card
PCC9560

MOTOROLA

series™

DUAL-BAND MOBILE TELEPHONE

New Packaging

- KAG TO DROP IN VISUALS UPON APPROVAL

MOTOROLA

series™

DUAL-BAND MOBILE TELEPHONE

After Sales Service

- General consumer helplines for pre & post sales enquiries (same No. as cellular & paging)
- 12 months warranty
- Helpline for advice on service policy

Model V.3688

GSM 900/1800 MHz

MOTOROLA

V. series™

DUAL-BAND MOBILE TELEPHONE

An Integrated Pan EMEA Advertising, PR and POS Campaign

- 30 second TV Commercial available to all markets from September
- New Print campaign featuring designs from Mathew Williamson (leading fashion designer) from October
- Specific market media (e.g. Use of buses during London Fashion week)
- Market specific PR activity focusing on driving awareness of new colours in a stylish and fashionable way
- Eye-catching POS and merchandising materials based on the print creative

Model V.3688
GSM 900/1800 MHz

MOTOROLA

series™

DUAL-BAND MOBILE TELEPHONE

Summary - Launch Plan

- Launch of 2 new colours
- New logo and graphic that builds on style and brand character of stylish, outgoing and trend setting
- New TV and Print campaign supported by heavyweight PR, POS and merchandising
- Product in market 30 September
- TV Commercial on air from September
- Print Campaign from October

Model V.3688
GSM 900/1800 MHz

MOTOROLA

series™

DUAL-BAND MOBILE TELEPHONE

V.small V.light V.desirable V.colours

Model V.3688

GSM 900/1800 MHz

Jack Colin-WCJ006
Sent: Friday, January 15, 1999 12:26 PM
To: Ray Collins
Subject: Kramer Complete BOM

SWF3076DA Bom Report

LVL COMPONENT_PART DESCRIPTION QTY C Q M D P

> 1 CDHN4286A KRAMER FLIP/FRNT HSG ASSY 1 1 1 M Y N
>
> 2 0104792Z01 ASSY XCVR FRNT HSNG 1 1 1 B Y N
>
> 3 0585627H01 GROMMET ALERT 1 2 1 B Y N
>
> 3 1504794Z01 HSNG FRNT XCVR 1 2 1 B Y N
>
> 3 3885765G02 BUTTON SMART 1 2 1 B Y N
>
> 2 0185763G01 ASSY FLIP 1 1 1 M Y Y
>
> 3 0103785K08 ASSY DISP/AUDIO LCD GSM 1 1 1 M Y Y
>
> 4 5003880S01 SPKR EM EARPC 15MM SMD 1 1 1 B Y N
>
> 4 6003710K04 BATT LI 3.3V COIN CELL 1 1 1 B Y N
>
> 4 7203908S03 LCD DSPL MOD 96X54 PIX W/HOLD 1 1 1 B Y N
>
> 4 7585766G01 PAD KRAMMER RTC 1 1 1 B Y N
>
> 3 0185895H01 ASSY FLIP REAR THICK BLK 1 1 1 B Y N
>
> 4 1585796H01 HOUSING FLIP REAR TICK 1 2 1 B Y N
>
> 4 5403796S02 LABEL FLIP FLEX BLK MOT 1 2 1 B Y N
>
> 4 5685640J01 LINER ESCUTCHEON 1 2 1 B Y N
>
> 3 0185896H01 ASSY FLIP FRNT BLK 1 1 1 B Y N
>
> 4 1509324T01 HSNG FRNT FLIP BLK 1 2 1 B Y N
>
> 4 3204567Z01 VADER SPKR FELT 1 2 1 B Y N
>
> 4 3209104C05 GASKET SPEAKER 1 2 1 B Y N
>
> 4 3209326T03 GASKET DISPLAY KRAMER 1 2 1 B Y N
>
> 4 5983583N18 MAGNET GSM RAE 1 2 1 B Y N
>
> 2 5504765Z02 HINGE MECHANISM BADAR 1 1 1 B Y N
>
> 3 0404742Z01 WASHER HINGE VADAR 1 2 1 B Y N
>

> 3 4104741Z01 SPRING HINGE VADAR 1 2 1 B Y N
>
> 3 4304764Z01 SPACER HINGE VADAR 1 2 1 B Y N
>
> 3 4504596Z01 CAM 1 2 1 B Y N
>
> 3 4504597Z02 CAM FOLLOWER HINGE KRAMER 1 2 1 B Y N
>
> 1 SHN6860A H&H MOTOROLA STARTAC 210 INIQU 1 1 1 M Y Y
>
> 2 0104793Z01 ASSY XCVR REAR HSNG 1 1 1 M Y N
>
> 3 0309147T03 SCREW INTERNAL FRNT CRICKET 1 2 1 B Y N
>
> 3 1503853K01 HSNG XCVR REAR 1 2 1 B Y N
>
> 3 3809440U01 BUTTON VOICE - IT 1 2 1 B Y N
>
> 3 4104539Z01 SPRING MECHANICAL CONTACT 2 2 1 B Y N
>
> 3 4109378U01 SPRING COMPRESSION 1 2 1 B Y N
>
> 3 4285952G03 CLIP VIBRATOR BRACKET 1 2 1 B Y N
>
> 3 4285953G05 CLIP VIBRATOR CONTACT 1 2 1 B Y N
>
> 3 5509377U01 LATCH BATTERY 1 2 1 B Y N
>
> 3 5909382K01 MOTOR VIB 6MM 1.3V 7.5KRPM 1 2 1 B Y N
>
> 2 6185833G02 LENS LCD 1 1 1 B Y N
>
> 1 SHN6861A H&H MOTOROLA STARTAC 210 COMMO 1 1 1 M Y Y
>
> 2 0185829G02 ASSY ANT STUBBY GSM 1 1 1 B Y N
>
> 2 0509380T01 VADER MIC GROMMET 1 1 1 B Y N
>
> 2 0585699J01 GROMMET MICROPHONE 1 4 1 B Y N
>
> 2 3809378T02 VADER KYPD 19 BUTTON GSM 1 1 1 B Y N
>
> 2 3809378T04 KYPD GSM 1 4 1 B Y N
>
> 2 4385720J01 SPACER FLEX KRAMER 1 1 1 B Y N
>
> 2 4385988H01 INSERT ANTENNA 1 1 1 B Y N
>
> 2 5009135L07 MIC ELECT 6MM PINS 1 1 1 B Y N
>
> 2 5402525T01 LABEL COMPOSITE TXCVR 1 2 1 B Y N
>
> 2 6185635H02 LIGHT GUIDE 1 1 1 B Y N
>
> 2 7585824J01 PAD CONNECTOR 1 1 1 B Y N
>

> 1 SWF3077DA XCVR (H12) STARTC 210 CORE BLK 1 1 1 M Y Y
>
> 2 CDLF1471T TEMP KRMR H12 ROM 3.1 XCVR BD 1 1 1 M Y N
>
> 3 0102467T30 TEMP KRAMER H12 TOP SIDE 1 1 1 M Y Y
>
> 4 (PRA2819) PRELIMINARY BILL OF MATERIAL 1 2 1 Y N
>
> 4 0609591M25 RES CHIP DUAL 1K 5% 0.63W 1 1 1 B Y N
> R302
> 4 0609591M37 RES CHIP DUAL 10K 5% 0.63W 1 1 1 B Y N
> R307
> 4 0609591M49 RES CHIP DUAL 100K 5% .63W 4 1 1 B Y N
> R800
> 4 RES CHIP DUAL 100K 5% .63W 1 1 B Y N
> R801
> 4 RES CHIP DUAL 100K 5% .63W 1 1 B Y N
> R802
> 4 RES CHIP DUAL 100K 5% .63W 1 1 B Y N
> R803
> Motorola Internal Use Only
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> SWF3076DA Bom Report
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> LVL COMPONENT_PART DESCRIPTION QTY C Q M D P
> REF
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> 4 0611079A02 RES FIXED CHIP 1 5 1/10 A/P 1 1 1 B Y N
> R972
> 4 0662057M01 RES. CHIP 0 5% 20X40 13 1 1 B Y N
> R940
> 4 RES. CHIP 0 5% 20X40 1 1 B Y N
> R941
> 4 RES. CHIP 0 5% 20X40 1 1 B Y N
> R999
> 4 RES. CHIP 0 5% 20X40 1 1 B Y N
> R732
> 4 RES. CHIP 0 5% 20X40 1 1 B Y N
> R735
> 4 RES. CHIP 0 5% 20X40 1 1 B Y N
> R737
> 4 RES. CHIP 0 5% 20X40 1 1 B Y N
> R290
> 4 RES. CHIP 0 5% 20X40 1 1 B Y N
> R316
> 4 RES. CHIP 0 5% 20X40 1 1 B Y N
> R944
> 4 RES. CHIP 0 5% 20X40 1 1 B Y N
> R948
> 4 RES. CHIP 0 5% 20X40 1 1 B Y N
> R931
> 4 RES. CHIP 0 5% 20X40 1 1 B Y N
> R926
> 4 RES. CHIP 0 5% 20X40 1 1 B Y N

> L338
> 4 0662057M26 RES. CHIP 10 5% 20X40 2 1 1 B Y N
> R1000
> 4 RES. CHIP 10 5% 20X40 1 1 B Y N
> R1001
> 4 0662057M38 RES CHIP 33 5% 20X40 5 1 1 B Y N
> R1002
> 4 RES CHIP 33 5% 20X40 1 1 B Y N
> R227
> 4 RES CHIP 33 5% 20X40 1 1 B Y N
> R228
> 4 RES CHIP 33 5% 20X40 1 1 B Y N
> R990
> 4 RES CHIP 33 5% 20X40 1 1 B Y N
> R705
> 4 0662057M50 RES. CHIP 100 5% 20X40 5 1 1 B Y N
> R241
> 4 RES. CHIP 100 5% 20X40 1 1 B Y N
> R909
> 4 RES. CHIP 100 5% 20X40 1 1 B Y N
> R910
> 4 RES. CHIP 100 5% 20X40 1 1 B Y N
> R710
> 4 RES. CHIP 100 5% 20X40 1 1 B Y N
> R711
> 4 0662057M52 RES. CHIP 120 5% 20X40 1 1 1 B Y N
> R806
> 4 0662057M54 RES. CHIP 150 5% 20X40 2 1 1 B Y N
> R973
> 4 RES. CHIP 150 5% 20X40 1 1 B Y N
> R974
> 4 0662057M58 RES. CHIP 220 5% 20X40 2 1 1 B Y N
> R344
> 4 RES. CHIP 220 5% 20X40 1 1 B Y N
> R1003
> 4 0662057M60 RES. CHIP 270 5% 20X40 1 1 1 B Y N
> R908
> 4 0662057M62 RES. CHIP 330 5% 20X40 1 1 1 B Y N
> R225
> 4 0662057M64 RES. CHIP 390 5% 20X40 1 1 1 B Y N
> R807
> 4 0662057M66 RES. CHIP 470 5% 20X40 2 1 1 B Y N
> R971
> 4 RES. CHIP 470 5% 20X40 1 1 B Y N
> R201
> 4 0662057M68 RES. CHIP 560 5% 20X40 2 1 1 B Y N
> R900
> 4 RES. CHIP 560 5% 20X40 1 1 B Y N
> R915
> 4 0662057M70 RES. CHIP 680 5% 20X40 3 1 1 B Y N
> R331
> 4 RES. CHIP 680 5% 20X40 1 1 B Y N
> R920
> 4 RES. CHIP 680 5% 20X40 1 1 B Y N
> R204
> 4 0662057M74 RES. CHIP 1000 5% 20X40 7 1 1 B Y N

> R226
> 4 RES. CHIP 1000 5% 20X40 1 1 B Y N
> R306
> 4 RES. CHIP 1000 5% 20X40 1 1 B Y N
> R309
> 4 RES. CHIP 1000 5% 20X40 1 1 B Y N
> R633
> 4 RES. CHIP 1000 5% 20X40 1 1 B Y N
> R330
> 4 RES. CHIP 1000 5% 20X40 1 1 B Y N
> R991
> 4 RES. CHIP 1000 5% 20X40 1 1 B Y N
> R328
> 4 0662057M76 RES. CHIP 1200 5% 20X40 2 1 1 B Y N
> R202
> 4 RES. CHIP 1200 5% 20X40 1 1 B Y N
> R222
> 4 0662057M82 RES. CHIP 2200 5% 20X40 3 1 1 B Y N
> R993
> 4 RES. CHIP 2200 5% 20X40 1 1 B Y N
> R118
> 4 RES. CHIP 2200 5% 20X40 1 1 B Y N
> R200
> 4 0662057M90 RES. CHIP 4700 5% 20X40 7 1 1 B Y N
> R343
> 4 RES. CHIP 4700 5% 20X40 1 1 B Y N
> R625
> 4 RES. CHIP 4700 5% 20X40 1 1 B Y N
> R635
> 4 RES. CHIP 4700 5% 20X40 1 1 B Y N
> R903
> 4 RES. CHIP 4700 5% 20X40 1 1 B Y N
> R943
> 4 RES. CHIP 4700 5% 20X40 1 1 B Y N
> R848
> 4 RES. CHIP 4700 5% 20X40 1 1 B Y N
> R238
> 4 0662057M92 RES. CHIP 5600 5% 20X40 1 1 1 B Y N
> R946
> Motorola Internal Use Only
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>
> SWF3076DA Bom Report
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> LVL COMPONENT_PART DESCRIPTION QTY C Q M D P
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> 4 0662057M96 RES. CHIP 8200 5% 20X40 1 1 1 B Y N
> R340
> 4 0662057M98 RES. CHIP 10K 5% 20X40 16 1 1 B Y N
> R223
> 4 RES. CHIP 10K 5% 20X40 1 1 B Y N
> R342
> 4 RES. CHIP 10K 5% 20X40 1 1 B Y N
> R627

> 4 RES. CHIP 10K 5% 20X40 1 1 B Y N
> R628
> 4 RES. CHIP 10K 5% 20X40 1 1 B Y N
> R305
> 4 RES. CHIP 10K 5% 20X40 1 1 B Y N
> R919
> 4 RES. CHIP 10K 5% 20X40 1 1 B Y N
> R230
> 4 RES. CHIP 10K 5% 20X40 1 1 B Y N
> R911
> 4 RES. CHIP 10K 5% 20X40 1 1 B Y N
> R620
> 4 RES. CHIP 10K 5% 20X40 1 1 B Y N
> R631
> 4 RES. CHIP 10K 5% 20X40 1 1 B Y N
> R301
> 4 RES. CHIP 10K 5% 20X40 1 1 B Y N
> R700
> 4 RES. CHIP 10K 5% 20X40 1 1 B Y N
> R703
> 4 RES. CHIP 10K 5% 20X40 1 1 B Y N
> R310
> 4 RES. CHIP 10K 5% 20X40 1 1 B Y N
> R312
> 4 RES. CHIP 10K 5% 20X40 1 1 B Y N
> R709
> 4 0662057N06 RES. CHIP 20K 5% 20X40 1 1 1 B Y N
> R632
> 4 0662057N07 RES. CHIP 22K 5% 20X40 2 1 1 B Y N
> R917
> 4 RES. CHIP 22K 5% 20X40 1 1 B Y N
> R308
> 4 0662057N09 RES. CHIP 27K 5% 20X40 2 1 1 B Y N
> R231
> 4 RES. CHIP 27K 5% 20X40 1 1 B Y N
> R259
> 4 0662057N11 RES. CHIP 33K 5% 20X40 2 1 1 B Y N
> R329
> 4 RES. CHIP 33K 5% 20X40 1 1 B Y N
> R304
> 4 0662057N12 RES. CHIP 36K 5% 20X40 1 1 1 B Y N
> R916
> 4 0662057N13 RES. CHIP 39K 5% 20X40 1 1 1 B Y N
> R258
> 4 0662057N23 RES. CHIP 100K 5% 20X40 9 1 1 B Y N
> R621
> 4 RES. CHIP 100K 5% 20X40 1 1 B Y N
> R622
> 4 RES. CHIP 100K 5% 20X40 1 1 B Y N
> R623
> 4 RES. CHIP 100K 5% 20X40 1 1 B Y N
> R624
> 4 RES. CHIP 100K 5% 20X40 1 1 B Y N
> R912
> 4 RES. CHIP 100K 5% 20X40 1 1 B Y N
> R205

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>       4            RES. CHIP 100K  5% 20X40          1 1 B Y N
> R206
>       4            RES. CHIP 100K  5% 20X40          1 1 B Y N
> R320
>       4            RES. CHIP 100K  5% 20X40          1 1 B Y N
> R341
>       4   0662057N27   RES. CHIP 150K  5% 20X40        1 1 1 B Y N
> R636
>       4   0662057N29   RES. CHIP 180K  5% 20X40        1 1 1 B Y N
> R950
>       4   0662057N32   RES. CHIP 240K  5% 20X40        1 1 1 B Y N
> R957
>       4   0662057N33   RES. CHIP 270K  5% 20X40        2 1 1 B Y N
> R942
>       4            RES. CHIP 270K  5% 20X40          1 1 B Y N
> R240
>       4   0662057N39   RES CHIP 470K 5% 20X40          5 1 1 B Y N
> R913
>       4            RES CHIP 470K 5% 20X40          1 1 B Y N
> R914
>       4            RES CHIP 470K 5% 20X40          1 1 B Y N
> R955
>       4            RES CHIP 470K 5% 20X40          1 1 B Y N
> R956
>       4            RES CHIP 470K 5% 20X40          1 1 B Y N
> R951
>       4   0662057N47   RES. CHIP 1.0 MEG  5% 20X40      1 1 1 B Y N
> R220
>       4   0903788K01   RECPT ZIF RT ANGL 27 CKT SMD     1 1 1 B Y N
>
>       4            RECPT ZIF RT ANGL 27 CKT SMD       1 1 B Y N
> J700
>       4   0909449B03   RECEPT MODULE 15 PIN SMD         1 1 1 B Y N
> J600
>       4   0985622G01   SKT TOP ENTRY 2 POS              1 1 1 B Y N
> J00910
>       4   2104801Z01   AP CER NPO 0.5PF 16V 1005 SMD    1 1 1 B Y N
> L103
>       4   2109622N06   CAP CER CHIP NPO CLASS I         1 1 1 B Y N
> C201
>       4   2109622N16   CAP CER CHIP NPO CLASS I         2 1 1 B Y N
> C220
>       4            CAP CER CHIP NPO CLASS I          1 1 B Y N
> C205
>       4   2113740A69   CAP CHIP REEL CL1 +/-30 390      1 1 1 B Y N
> C221
>       4   2113740F63   CAP CHIP CL1 +/-30 330  5%       1 1 1 B Y N
> C200
>       4   2113741F28   CAP CHIP CL2 X7R REEL 1300       1 1 1 B Y N
> C231
>       4   2113741F33   CAP CHIP CL2 X7R REEL 2200       1 1 1 B Y N
> C290
>       4   2113741M17   CAP CHIP CL2 X7R 10% 680         1 1 1 B Y N
> C260
>       4   2113743E07   CER CHIP CAP .022UF              2 1 1 B Y N
> C916
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>        4              CER CHIP CAP .022UF               1 1 B Y N
> C917
>                     Motorola Internal Use Only
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>
>                       SWF3076DA Bom Report
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>      LVL COMPONENT_PART  DESCRIPTION                  QTY C Q M D P
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>        4   2113743G21   CER CHIP CAP 1.0 UF             3 1 1 B Y N
> C243
>        4              CER CHIP CAP 1.0 UF               1 1 B Y N
> C245
>        4              CER CHIP CAP 1.0 UF               1 1 B Y N
> C239
>        4   2113743H14   CAP CHIP 10.0 UF 16V +80-20%     6 1 1 B Y N
> C923
>        4              CAP CHIP 10.0 UF 16V +80-20%      1 1 B Y N
> C924
>        4              CAP CHIP 10.0 UF 16V +80-20%      1 1 B Y N
> C926
>        4              CAP CHIP 10.0 UF 16V +80-20%      1 1 B Y N
> C927
>        4              CAP CHIP 10.0 UF 16V +80-20%      1 1 B Y N
> C946
>        4              CAP CHIP 10.0 UF 16V +80-20%      1 1 B Y N
> C945
>        4   2113743L01   CAP CHIP 220 PF 10% X7R         1 1 1 B Y N
> C341
>        4   2113743L03   CAP CHIP 270 PF 10% X7R         1 1 1 B Y N
> C348
>        4   2113743L05   CAP CHIP 330 PF 10% X7R         1 1 1 B Y N
> C345
>        4   2113743L17   CAP CHIP 1000 PF 10% X7R        6 1 1 B Y N
> C123
>        4              CAP CHIP 1000 PF 10% X7R          1 1 B Y N
> C223
>        4              CAP CHIP 1000 PF 10% X7R          1 1 B Y N
> C270
>        4              CAP CHIP 1000 PF 10% X7R          1 1 B Y N
> C950
>        4              CAP CHIP 1000 PF 10% X7R          1 1 B Y N
> C332
>        4              CAP CHIP 1000 PF 10% X7R          1 1 B Y N
> C346
>        4   2113743L41   CAP CHIP 10000 PF 10% X7R       10 1 1 B Y N
> C230
>        4              CAP CHIP 10000 PF 10% X7R         1 1 B Y N
> C241
>        4              CAP CHIP 10000 PF 10% X7R         1 1 B Y N
> C246
>        4              CAP CHIP 10000 PF 10% X7R         1 1 B Y N
> C229
>        4              CAP CHIP 10000 PF 10% X7R         1 1 B Y N
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> C247
> 4 CAP CHIP 10000 PF 10% X7R 1 1 B Y N
> C963
> 4 CAP CHIP 10000 PF 10% X7R 1 1 B Y N
> C334
> 4 CAP CHIP 10000 PF 10% X7R 1 1 B Y N
> C620
> 4 CAP CHIP 10000 PF 10% X7R 1 1 B Y N
> C621
> 4 CAP CHIP 10000 PF 10% X7R 1 1 B Y N
> C965
> 4 2113743M24 CAP CHIP 100000 PF +80-20% Y5V 9 1 1 B Y N
> C919
> 4 CAP CHIP 100000 PF +80-20% Y5V 1 1 B Y N
> C920
> 4 CAP CHIP 100000 PF +80-20% Y5V 1 1 B Y N
> C1259
> 4 CAP CHIP 100000 PF +80-20% Y5V 1 1 B Y N
> C219
> 4 CAP CHIP 100000 PF +80-20% Y5V 1 1 B Y N
> C225
> 4 CAP CHIP 100000 PF +80-20% Y5V 1 1 B Y N
> C723
> 4 CAP CHIP 100000 PF +80-20% Y5V 1 1 B Y N
> C991
> 4 CAP CHIP 100000 PF +80-20% Y5V 1 1 B Y N
> C724
> 4 CAP CHIP 100000 PF +80-20% Y5V 1 1 B Y N
> C932
> 4 2113743N07 CAP CHIP 1.5 PF +-.25PF COG 1 1 1 B Y N
> C00994
> 4 2113743N14 CAP CHIP 3.3 PF +-.25PF COG 2 1 1 B Y N
> C00339
> 4 CAP CHIP 3.3 PF +-.25PF COG 1 1 B Y N
> C01268
> 4 2113743N16 CAP CHIP 3.9 PF +-.25PF COG 1 1 1 B Y N
> C338
> 4 2113743N18 CAP CHIP 4.7 PF +-.25PF COG 1 1 1 B Y N
> C266
> 4 2113743N20 CAP CHIP 5.6 PF + -.5PF COG 2 1 1 B Y N
> C967
> 4 CAP CHIP 5.6 PF + -.5PF COG 1 1 B Y N
> C968
> 4 2113743N24 CAP CHIP 8.2 PF + -.5PF COG 4 1 1 B Y N
> C259
> 4 CAP CHIP 8.2 PF + -.5PF COG 1 1 B Y N
> C970
> 4 CAP CHIP 8.2 PF + -.5PF COG 1 1 B Y N
> C330
> 4 CAP CHIP 8.2 PF + -.5PF COG 1 1 B Y N
> C336
> 4 2113743N26 CAP CHIP 10.0 PF 5% COG 4 1 1 B Y N
> C331
> 4 CAP CHIP 10.0 PF 5% COG 1 1 B Y N
> C705
> 4 CAP CHIP 10.0 PF 5% COG 1 1 B Y N

> C335
> 4 CAP CHIP 10.0 PF 5% COG 1 1 B Y N
> C244
> 4 CAP CHIP 10.0 PF 5% COG 14 1 1 B Y N
> C730
> 4 CAP CHIP 10.0 PF 5% COG 1 1 B Y N
> C731
> 4 CAP CHIP 10.0 PF 5% COG 1 1 B Y N
> C732
> 4 CAP CHIP 10.0 PF 5% COG 1 1 B Y N
> C733
> 4 CAP CHIP 10.0 PF 5% COG 1 1 B Y N
> C734
> 4 CAP CHIP 10.0 PF 5% COG 1 1 B Y N
> C735
> 4 CAP CHIP 10.0 PF 5% COG 1 1 B Y N
> C736
> 4 CAP CHIP 10.0 PF 5% COG 1 1 B Y N
> C737
> 4 CAP CHIP 10.0 PF 5% COG 1 1 B Y N
> C738
> Motorola Internal Use Only
>
>
> SWF3076DA Bom Report
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> LVL COMPONENT_PART DESCRIPTION QTY C Q M D P
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> 4 2113743N26 CAP CHIP 10.0 PF 5% COG 14 1 1 B Y N
> C739
> 4 CAP CHIP 10.0 PF 5% COG 1 1 B Y N
> C740
> 4 CAP CHIP 10.0 PF 5% COG 1 1 B Y N
> C741
> 4 CAP CHIP 10.0 PF 5% COG 1 1 B Y N
> C742
> 4 CAP CHIP 10.0 PF 5% COG 1 1 B Y N
> C743
> 4 2113743N28 CAP CHIP 12.0 PF 5% COG 1 1 1 B Y N
> R224
> 4 2113743N30 CAP CHIP 15.0 PF 5% COG 2 1 1 B Y N
> C236
> 4 CAP CHIP 15.0 PF 5% COG 1 1 B Y N
> C1266
> 4 2113743N34 CAP CHIP 22.0 PF 5% COG 5 1 1 B Y N
> C349
> 4 CAP CHIP 22.0 PF 5% COG 1 1 B Y N
> C340
> 4 CAP CHIP 22.0 PF 5% COG 1 1 B Y N
> C344
> 4 CAP CHIP 22.0 PF 5% COG 1 1 B Y N
> C347
> 4 CAP CHIP 22.0 PF 5% COG 1 1 B Y N
> C292

> 4 2113743N36 CAP CHIP 27.0 PF 5% COG 6 1 1 B Y N
> C333
> 4 CAP CHIP 27.0 PF 5% COG 1 1 B Y N
> C101
> 4 CAP CHIP 27.0 PF 5% COG 1 1 B Y N
> C453
> 4 CAP CHIP 27.0 PF 5% COG 1 1 B Y N
> C459
> 4 CAP CHIP 27.0 PF 5% COG 1 1 B Y N
> C992
> 4 CAP CHIP 27.0 PF 5% COG 1 1 B Y N
> C117
> 4 2113743N38 CAP CHIP 33.0 PF 5% COG 11 1 1 B Y N
> C903
> 4 CAP CHIP 33.0 PF 5% COG 1 1 B Y N
> C912
> 4 CAP CHIP 33.0 PF 5% COG 1 1 B Y N
> C954
> 4 CAP CHIP 33.0 PF 5% COG 1 1 B Y N
> C955
> 4 CAP CHIP 33.0 PF 5% COG 1 1 B Y N
> C956
> 4 CAP CHIP 33.0 PF 5% COG 1 1 B Y N
> C957
> 4 CAP CHIP 33.0 PF 5% COG 1 1 B Y N
> C106
> 4 CAP CHIP 33.0 PF 5% COG 1 1 B Y N
> C802
> 4 CAP CHIP 33.0 PF 5% COG 1 1 B Y N
> C610
> 4 CAP CHIP 33.0 PF 5% COG 1 1 B Y N
> C611
> 4 CAP CHIP 33.0 PF 5% COG 1 1 B Y N
> C343
> 4 2113743N40 CAP CHIP 39.0 PF 5% COG 5 1 1 B Y N
> C237
> 4 CAP CHIP 39.0 PF 5% COG 1 1 B Y N
> C238
> 4 CAP CHIP 39.0 PF 5% COG 1 1 B Y N
> C601
> 4 CAP CHIP 39.0 PF 5% COG 1 1 B Y N
> C602
> 4 CAP CHIP 39.0 PF 5% COG 1 1 B Y N
> C603
> 4 2113743N42 CAP CHIP 47.0 PF 5% COG 1 1 1 B Y N
> C305
> 4 2113743N44 CAP CHIP 56.0 PF 5% COG 1 1 1 B Y N
> C969
> 4 2113743N50 CAP CHIP 100 PF 5% COG 4 1 1 B Y N
> C111
> 4 CAP CHIP 100 PF 5% COG 1 1 B Y N
> C226
> 4 CAP CHIP 100 PF 5% COG 1 1 B Y N
> C114
> 4 CAP CHIP 100 PF 5% COG 1 1 B Y N
> C342

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>        4    2113743N52   CAP CHIP 120 PF 5% COG           3 1 1 B Y N
> C224
>        4              CAP CHIP 120 PF 5% COG             1 1 B Y N
> C227
>        4              CAP CHIP 120 PF 5% COG             1 1 B Y N
> C232
>        4    2113928J08   CAP CERAMIC CHIP 10.0UF          1 1 1 B Y N
> C941
>        4    2113928P04   CAP CER CHIP 1.0UF 20% 6.3V      2 1 1 B Y N
> C911
>        4              CAP CER CHIP 1.0UF 20% 6.3V        1 1 B Y N
> C906
>        4    2309109S02   CAP TANT 68UF 10% 10V 7343L      1 1 1 B Y N
> C934
>        4    2311049A07   CAP TANT CHIP 1 10 16 A/P        2 1 1 B Y N
> C240
>        4              CAP TANT CHIP 1 10 16 A/P          1 1 B Y N
> C242
>        4    2311049A56   CAP TAN CHIP A/P 4.7 20 10       1 1 1 B Y N
> C904
>        4    2311049C18   CAP TANT CHIP 4.7UF  6V 10%      1 1 1 B Y N
> C801
>        4    2311049C21   CAP TANT CHIP 3.3UF 10V 10%      1 1 1 B Y N
> C947
>        4    2404554Z27   IND MTLY 8.2 UH 10 1608 SHLD     1 1 1 B Y N
> L230
>        4    2404554Z28   IND MTLY 10UH 10 1608 SHLD       1 1 1 B Y N
> L290
>        4    2409092R07   IND CHIP PWR 1008 10 UH SMD      1 1 1 B Y N
> L240
>        4    2409154M04   IND CER MLTILYR 1.8NH 1005       1 1 1 B Y N
> C103
>        4    2409154M83   IND CER MLTILYR 3.9 NH 1005      1 1 1 B Y N
> L00339
>        4    2409154M88   IND CER MLTILYR 10.0NH 1005      1 1 1 B Y N
> L990
>        4    2409154M96   IND CER MLTILYR 47.0NH 1005      1 1 1 B Y N
> L123
>        4    2409646M53   IN CER MULTILYR 5.6NH 1608       1 1 1 B Y N
> L259
>                      Motorola Internal Use Only
>
>
>                        SWF3076DA Bom Report
>
>       LVL COMPONENT_PART  DESCRIPTION                   QTY C Q M D P
> REF
> ---------- --------------- ------------------------------ ---- - - - - -
> ------
>        4    2503778K07   CHK 15UH 0.4 HM 5X6MM SMD        1 1 1 B Y N
> L901
>        4    2603864K02   SHIELD MAGIC                     1 1 1 B Y N
> SH900
>        4    3909426M01   CNTCT BLK SIM CARD READER ZAP     1 1 1 B Y N
> J900
>        4    3985737G01   CNTCT BLCK 4 CKT                 1 1 1 B Y N
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> J604
> 4 4009368L03 SW TACTILE RT ANGL 3 POLE SMD 1 1 1 B Y N
> VA
> 4 4209388S01 CLIP TOP FLEX 2 1 1 B Y N
> J810
> 4 CLIP TOP FLEX 1 1 B Y N
> J811
> 4 4809118D02 LED BICOLOR LNJ115W8POMT 1 1 1 B Y N
> CR806
> 4 4809527E24 TSTR NPN RF MRF949LT1 SC-90 1 1 1 B Y N
> Q1255
> 4 4809579E02 TSTR MOSFET N-CHAN 25K1830 2 1 1 B Y N
> Q960
> 4 TSTR MOSFET N-CHAN 25K1830 1 1 B Y N
> Q950
> 4 4809579E18 TSTR MOSFET P-CHAN TP0101T 2 1 1 B Y N
> Q240
> 4 TSTR MOSFET P-CHAN TP0101T 1 1 B Y N
> Q242
> 4 4809579E24 TSTR FET P-CHAN 2SJ347 SC90 1 1 1 B Y N
> Q628
> 4 4809579E29 TSTR FET P-CHAN SI3443DV 6TSOP 1 1 1 B Y N
> Q901
> 4 4809579E30 TSTR FET DUAL N-CHAN HN1K02FU 2 1 1 B Y N
> Q805
> 4 TSTR FET DUAL N-CHAN HN1K02FU 1 1 B Y N
> Q241
> 4 4809605E02 TSTR SIG NPN 2SC4617 1 1 1 B Y N
> Q912
> 4 4809606E02 DIODE DUAL ARRAY DAN222 1 1 1 B Y N
> CR920
> 4 4809607E02 TSTR SIG PNP 25A1774 2 1 1 B Y N
> Q320
> 4 TSTR SIG PNP 25A1774 1 1 B Y N
> Q635
> 4 4809608E03 TSTR DIG PNP DTA114YE 2 1 1 B Y N
> Q803
> 4 TSTR DIG PNP DTA114YE 1 1 B Y N
> Q322
> 4 4809612J22 XTAL 26MHZ 11PPM 6X8.5MM SMD 1 1 1 B Y N
> Y230
> 4 4809653F07 RECT SCHTTKY 1A MBRM120ET3 3 1 1 B Y N
> CR910
> 4 RECT SCHTTKY 1A MBRM120ET3 1 1 B Y N
> CR901
> 4 RECT SCHTTKY 1A MBRM120ET3 1 1 B Y N
> CR940
> 4 4809807C24 TSTR FET P-CHAN 2.5W SI4463DY 2 1 1 B Y N
> Q330
> 4 TSTR FET P-CHAN 2.5W SI4463DY 1 1 B Y N
> Q942
> 4 4809877C09 DIODE VARACTOR BB555 ESC 1 1 1 B Y N
> CR259
> 4 4809877C10 DIODE VARACTOR BB659 ESC 1 1 1 B Y N
> CR230
> 4 4809939C05 TSTR DUAL NPN/PNP UMH 5 2 1 1 B Y N

> Q340
> 4 TSTR DUAL NPN/PNP UMH 5 1 1 B Y N
> Q343
> 4 4809939C06 TSTR DUAL PNP/NPN UMZ2N 3 1 1 B Y N
> Q902
> 4 TSTR DUAL PNP/NPN UMZ2N 1 1 B Y N
> Q302
> 4 TSTR DUAL PNP/NPN UMZ2N 1 1 B Y N
> Q304
> 4 4809939C07 TSTR DUAL PNP/PNP UMA4NTL 2 1 1 B Y N
> Q333
> 4 TSTR DUAL PNP/PNP UMA4NTL 1 1 B Y N
> Q342
> 4 4809939C08 TSTR DUAL PNP/PNP UMA6NTL 1 1 1 B Y N
> Q201
> 4 4809939C09 TSTR DUAL NPN/NPN UMH4 3 1 1 B Y N
> Q301
> 4 TSTR DUAL NPN/NPN UMH4 1 1 B Y N
> Q202
> 4 TSTR DUAL NPN/NPN UMH4 1 1 B Y N
> Q331
> 4 4809939C12 TSTR DUAL NPN/NPN UPA806T-T1 1 1 1 B Y N
> Q303
> 4 4809940E02 TSTR DIG NPN DTC114YE 1 1 1 B Y N
> Q321
> 4 4809940E03 TSTR DIG NPN DTC114TE 1 1 1 B Y N
> Q911
> 4 4809948D15 DI0DE DUAL TVS 12V SM12 SOT23 1 1 1 B Y N
> CR942
> 4 4809948D16 DIODE QUAL TVS 12V SMS12 SOT23 1 1 1 B Y N
> VS944
> 4 4809948D18 DIODE QUAL TVS 5V SMS05 SOT23 1 1 1 B Y N
> CR948
> 4 5109512F14 IC VOLT REG 1.3V MM1426XNLE 1 1 1 B Y N
> U801
> 4 5109522E23 IC SNGL INV GATE TC7SH04FU 1 1 1 B Y N
> U00201
> 4 5109572E24 IC RF PA 5-PORT 3W 10MSOP 1 1 1 B Y N
> U101
> 4 5109632D91 IC CUST PAC SC79948DTB 14TSSOP 1 1 1 B Y N
> U340
> 4 5109731C28 IC OP AMP RR SOT 23 1 1 1 B Y N
> U200
> 4 5109817F26 IC VOLT DECT 2.9V TCVN2902ECB 1 1 1 B Y N
> Q710
> 4 5109817F30 IC COMPTR LMV331M 5SC70 1 1 1 B Y N
> U00950
> 4 5109817F31 VOLT DECT 2.8V PST995PUR 1 1 1 B Y N
> U341
> 4 5109879E28 IC BICOM MAGIC 2.6 80 BGA 1 1 1 B Y N
> U913
> 4 5109920D22 IC DC-DC CONV TCM828 SOT23A5 1 4 1 B Y N
> U901
> 4 5109920D35 IC VOLT CONV TC1229 SOT23A-6 1 1 1 B Y N
> U901
> 3 0102467T31 TEMP KRAMER H12 BOT ROM 3.1 1 1 1 M Y Y

>
> 4 (PRA2819) PRELIMINARY BILL OF MATERIAL 1 2 1 Y N
>
> Motorola Internal Use Only
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>
> SWF3076DA Bom Report
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> LVL COMPONENT_PART DESCRIPTION QTY C Q M D P
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> 4 0609175L02 RES CHIP 0.25 1% .25W 1206 1 1 1 B Y N
> R932
> 4 0660076S01 RES CHIP O OHM 1 1 1 B Y N
> L483
> 4 0662057M01 RES. CHIP 0 5% 20X40 8 1 1 B Y N
> R721
> 4 RES. CHIP 0 5% 20X40 1 1 B Y N
> R720
> 4 RES. CHIP 0 5% 20X40 1 1 B Y N
> R267
> 4 RES. CHIP 0 5% 20X40 1 1 B Y N
> R949
> 4 RES. CHIP 0 5% 20X40 1 1 B Y N
> R319
> 4 RES. CHIP 0 5% 20X40 1 1 B Y N
> R960
> 4 RES. CHIP 0 5% 20X40 1 1 B Y N
> R961
> 4 RES. CHIP 0 5% 20X40 1 1 B Y N
> R352
> 4 0662057M26 RES. CHIP 10 5% 20X40 1 1 1 B Y N
> R933
> 4 0662057M30 RES. CHIP 15 5% 20X40 3 1 1 B Y N
> R454
> 4 RES. CHIP 15 5% 20X40 1 1 B Y N
> R458
> 4 RES. CHIP 15 5% 20X40 1 1 B Y N
> R322
> 4 0662057M32 RES. CHIP 18 5% 20X40 1 1 1 B Y N
> R264
> 4 0662057M34 RES. CHIP 22 5% 20X40 1 1 1 B Y N
> R255
> 4 0662057M38 RES CHIP 33 5% 20X40 1 1 1 B Y N
> R712
> 4 0662057M43 RES. CHIP 51 5% 20X40 3 1 1 B Y N
> R254
> 4 RES. CHIP 51 5% 20X40 1 1 B Y N
> R300
> 4 RES. CHIP 51 5% 20X40 1 1 B Y N
> R326
> 4 0662057M46 RES. CHIP 68 5% 20X40 2 1 1 B Y N
> R261
> 4 RES. CHIP 68 5% 20X40 1 1 B Y N
> R980

> 4 0662057M48 RES. CHIP 82 5% 20X40 1 1 1 B Y N
> R266
> 4 0662057M50 RES. CHIP 100 5% 20X40 7 1 1 B Y N
> R350
> 4 RES. CHIP 100 5% 20X40 1 1 B Y N
> R1259
> 4 RES. CHIP 100 5% 20X40 1 1 B Y N
> R356
> 4 RES. CHIP 100 5% 20X40 1 1 B Y N
> R321
> 4 RES. CHIP 100 5% 20X40 1 1 B Y N
> R468
> 4 RES. CHIP 100 5% 20X40 1 1 B Y N
> R400
> 4 RES. CHIP 100 5% 20X40 1 1 B Y N
> R407
> 4 0662057M56 RES. CHIP 180 5% 20X40 1 1 1 B Y N
> R479
> 4 0662057M58 RES. CHIP 220 5% 20X40 3 1 1 B Y N
> R268
> 4 RES. CHIP 220 5% 20X40 1 1 B Y N
> R325
> 4 RES. CHIP 220 5% 20X40 1 1 B Y N
> R327
> 4 0662057M60 RES. CHIP 270 5% 20X40 1 1 1 B Y N
> R252
> 4 0662057M62 RES. CHIP 330 5% 20X40 4 1 1 B Y N
> R1262
> 4 RES. CHIP 330 5% 20X40 1 1 B Y N
> R476
> 4 RES. CHIP 330 5% 20X40 1 1 B Y N
> R303
> 4 RES. CHIP 330 5% 20X40 1 1 B Y N
> R0269
> 4 0662057M66 RES. CHIP 470 5% 20X40 1 1 1 B Y N
> R207
> 4 0662057M68 RES. CHIP 560 5% 20X40 4 1 1 B Y N
> R906
> 4 RES. CHIP 560 5% 20X40 1 1 B Y N
> R907
> 4 RES. CHIP 560 5% 20X40 1 1 B Y N
> R982
> 4 RES. CHIP 560 5% 20X40 1 1 B Y N
> R488
> 4 0662057M74 RES. CHIP 1000 5% 20X40 7 1 1 B Y N
> R462
> 4 RES. CHIP 1000 5% 20X40 1 1 B Y N
> R981
> 4 RES. CHIP 1000 5% 20X40 1 1 B Y N
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> 4 RES. CHIP 1000 5% 20X40 1 1 B Y N
> R311
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> R324
> 4 RES. CHIP 1000 5% 20X40 1 1 B Y N
> R00492

> 4 RES. CHIP 1000 5% 20X40 1 1 B Y N
> R253
> 4 0662057M76 RES. CHIP 1200 5% 20X40 1 1 1 B Y N
> R250
> 4 0662057M78 RES. CHIP 1500 5% 20X40 3 1 1 B Y N
> R351
> 4 RES. CHIP 1500 5% 20X40 1 1 B Y N
> R406
> 4 RES. CHIP 1500 5% 20X40 1 1 B Y N
> R271
> 4 0662057M81 RES. CHIP 2000 5% 20X40 1 1 1 B Y N
> R251
> 4 0662057M82 RES. CHIP 2200 5% 20X40 4 1 1 B Y N
> R1257
> 4 RES. CHIP 2200 5% 20X40 1 1 B Y N
> R477
> 4 RES. CHIP 2200 5% 20X40 1 1 B Y N
> R323
> 4 RES. CHIP 2200 5% 20X40 1 1 B Y N
> R490
> 4 0662057M84 RES. CHIP 2700 5% 20X40 3 1 1 B Y N
> R478
> Motorola Internal Use Only
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>
> SWF3076DA Bom Report
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> 4 0662057M84 RES. CHIP 2700 5% 20X40 3 1 1 B Y N
> R491
> 4 RES. CHIP 2700 5% 20X40 1 1 B Y N
> R1258
> 4 0662057M86 RES. CHIP 3300 5% 20X40 4 1 1 B Y N
> R262
> 4 RES. CHIP 3300 5% 20X40 1 1 B Y N
> R927
> 4 RES. CHIP 3300 5% 20X40 1 1 B Y N
> R221
> 4 RES. CHIP 3300 5% 20X40 1 1 B Y N
> R1261
> 4 0662057M88 RES. CHIP 3900 5% 20X40 1 1 1 B Y N
> R923
> 4 0662057M90 RES. CHIP 4700 5% 20X40 9 1 1 B Y N
> R263
> 4 RES. CHIP 4700 5% 20X40 1 1 B Y N
> R114
> 4 RES. CHIP 4700 5% 20X40 1 1 B Y N
> R451
> 4 RES. CHIP 4700 5% 20X40 1 1 B Y N
> R461
> 4 RES. CHIP 4700 5% 20X40 1 1 B Y N
> R115
> 4 RES. CHIP 4700 5% 20X40 1 1 B Y N

> R702
> 4 RES. CHIP 4700 5% 20X40 1 1 B Y N
> R921
> 4 RES. CHIP 4700 5% 20X40 1 1 B Y N
> R01260
> 4 RES. CHIP 4700 5% 20X40 1 1 B Y N
> R804
> 4 0662057M92 RES. CHIP 5600 5% 20X40 2 1 1 B Y N
> R450
> 4 RES. CHIP 5600 5% 20X40 1 1 B Y N
> R460
> 4 0662057M98 RES. CHIP 10K 5% 20X40 5 1 1 B Y N
> R112
> 4 RES. CHIP 10K 5% 20X40 1 1 B Y N
> R117
> 4 RES. CHIP 10K 5% 20X40 1 1 B Y N
> R985
> 4 RES. CHIP 10K 5% 20X40 1 1 B Y N
> R704
> 4 RES. CHIP 10K 5% 20X40 1 1 B Y N
> R902
> 4 0662057N03 RES. CHIP 15K 5% 20X40 2 1 1 B Y N
> R750
> 4 RES. CHIP 15K 5% 20X40 1 1 B Y N
> R922
> 4 0662057N07 RES. CHIP 22K 5% 20X40 1 1 1 B Y N
> R924
> 4 0662057N09 RES. CHIP 27K 5% 20X40 2 1 1 B Y N
> R905
> 4 RES. CHIP 27K 5% 20X40 1 1 B Y N
> R708
> 4 0662057N12 RES. CHIP 36K 5% 20X40 1 1 1 B Y N
> R983
> 4 0662057N15 RES. CHIP 47K 5% 20X40 2 1 1 B Y N
> R706
> 4 RES. CHIP 47K 5% 20X40 1 1 B Y N
> R988
> 4 0662057N17 RES. CHIP 56K 5% 20X40 1 1 1 B Y N
> R984
> 4 0662057N19 RES. CHIP 68K 5% 20X40 2 1 1 B Y N
> R904
> 4 RES. CHIP 68K 5% 20X40 1 1 B Y N
> R987
> 4 0662057N23 RES. CHIP 100K 5% 20X40 2 1 1 B Y N
> R901
> 4 RES. CHIP 100K 5% 20X40 1 1 B Y N
> R929
> 4 0662057N27 RES. CHIP 150K 5% 20X40 1 1 1 B Y N
> R116
> 4 0662057N32 RES. CHIP 240K 5% 20X40 1 1 1 B Y N
> R989
> 4 0662057N33 RES. CHIP 270K 5% 20X40 2 1 1 B Y N
> R928
> 4 RES. CHIP 270K 5% 20X40 1 1 B Y N
> R701
> 4 0985839G01 JACK MOD 2.5MM PLUG SMD 1 1 1 B Y N

> J650
> 4 2104801Z01 AP CER NPO 0.5PF 16V 1005 SMD 1 1 1 B Y N
> C254
> 4 2104801Z03 CAP CER NPO 0.7PF 16V 1005 SMD 1 1 1 B Y N
> C493
> 4 2104801Z10 CAP CER NPO 1.5PF 16V 1005 SMD 2 1 1 B Y N
> C252
> 4 CAP CER NPO 1.5PF 16V 1005 SMD 1 1 B Y N
> C253
> 4 2104801Z16 CAP CER NPO 2.7PF 16V 1005 SMD 1 1 1 B Y N
> C258
> 4 2113740F25 CAP CHIP REEL CL1 +/-30 8.2 1 1 1 B Y N
> C308
> 4 2113740F43 CAP CHIP REEL CL1 +/-30 47.0 1 1 1 B Y N
> C202
> 4 2113740F51 CAP CHIP REEL CL1 +/-30 100.0 1 1 1 B Y N
>
> 4 2113740F58 CAP CHIP REEL CL1 +/-30 200 1 1 1 B Y N
> L112
> 4 2113740F61 CAP CHIP REEL CL1 +/130 270 1 1 1 B Y N
> C251
> 4 2113742C30 CAP CER CHP 4.7PF +-.25PF 100V 1 1 1 B Y N
> C309
> 4 2113743E03 CER CHIP CAP .015UF 1 1 1 B Y N
> C925
> 4 2113743E11 CAP CHIP .039 UF 10% X7R 1 1 1 B Y N
> C939
> 4 2113743E20 CAP CHIP .10 UF 10% 2 1 1 B Y N
> C951
> 4 CAP CHIP .10 UF 10% 1 1 B Y N
> C706
> 4 2113743L17 CAP CHIP 1000 PF 10% X7R 14 1 1 B Y N
> C250
> 4 CAP CHIP 1000 PF 10% X7R 1 1 B Y N
> C261
> 4 CAP CHIP 1000 PF 10% X7R 1 1 B Y N
> C356
> 4 CAP CHIP 1000 PF 10% X7R 1 1 B Y N
> C358
> 4 CAP CHIP 1000 PF 10% X7R 1 1 B Y N
> C311
> Motorola Internal Use Only
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> SWF3076DA Bom Report
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> 4 2113743L17 CAP CHIP 1000 PF 10% X7R 14 1 1 B Y N
> C313
> 4 CAP CHIP 1000 PF 10% X7R 1 1 B Y N
> C401
> 4 CAP CHIP 1000 PF 10% X7R 1 1 B Y N
> C487

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>       4             CAP CHIP 1000 PF 10% X7R          1 1 B Y N
> C354
>       4             CAP CHIP 1000 PF 10% X7R          1 1 B Y N
> C406
>       4             CAP CHIP 1000 PF 10% X7R          1 1 B Y N
> C467
>       4             CAP CHIP 1000 PF 10% X7R          1 1 B Y N
> C966
>       4             CAP CHIP 1000 PF 10% X7R          1 1 B Y N
> C407
>       4             CAP CHIP 1000 PF 10% X7R          1 1 B Y N
> C357
>       4   2113743L21   CAP CHIP 1500 PF 10% X7R         1 1 1 B Y N
> C921
>       4   2113743L41   CAP CHIP 10000 PF 10% X7R        4 1 1 B Y N
> C488
>       4             CAP CHIP 10000 PF 10% X7R         1 1 B Y N
> C495
>       4             CAP CHIP 10000 PF 10% X7R         1 1 B Y N
> C704
>       4             CAP CHIP 10000 PF 10% X7R         1 1 B Y N
> C937
>       4   2113743M24   CAP CHIP 100000 PF +80-20% Y5V   21 1 1 B Y N
> C701
>       4             CAP CHIP 100000 PF +80-20% Y5V     1 1 B Y N
> C702
>       4             CAP CHIP 100000 PF +80-20% Y5V     1 1 B Y N
> C922
>       4             CAP CHIP 100000 PF +80-20% Y5V     1 1 B Y N
> C710
>       4             CAP CHIP 100000 PF +80-20% Y5V     1 1 B Y N
> C711
>       4             CAP CHIP 100000 PF +80-20% Y5V     1 1 B Y N
> C713
>       4             CAP CHIP 100000 PF +80-20% Y5V     1 1 B Y N
> C714
>       4             CAP CHIP 100000 PF +80-20% Y5V     1 1 B Y N
> C900
>       4             CAP CHIP 100000 PF +80-20% Y5V     1 1 B Y N
> C901
>       4             CAP CHIP 100000 PF +80-20% Y5V     1 1 B Y N
> C905
>       4             CAP CHIP 100000 PF +80-20% Y5V     1 1 B Y N
> C907
>       4             CAP CHIP 100000 PF +80-20% Y5V     1 1 B Y N
> C908
>       4             CAP CHIP 100000 PF +80-20% Y5V     1 1 B Y N
> C712
>       4             CAP CHIP 100000 PF +80-20% Y5V     1 1 B Y N
> C715
>       4             CAP CHIP 100000 PF +80-20% Y5V     1 1 B Y N
> C716
>       4             CAP CHIP 100000 PF +80-20% Y5V     1 1 B Y N
> C717
>       4             CAP CHIP 100000 PF +80-20% Y5V     1 1 B Y N
> C718
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>       4            CAP CHIP 100000 PF +80-20% Y5V      1 1 B Y N
> C719
>       4            CAP CHIP 100000 PF +80-20% Y5V      1 1 B Y N
> C720
>       4            CAP CHIP 100000 PF +80-20% Y5V      1 1 B Y N
> C902
>       4            CAP CHIP 100000 PF +80-20% Y5V      1 1 B Y N
> CNEW
>       4   2113743N03   CAP CHIP 1.0 PF +-.25PF COG       4 1 1 B Y N
> C482
>       4            CAP CHIP 1.0 PF +-.25PF COG         1 1 B Y N
> C454
>       4            CAP CHIP 1.0 PF +-.25PF COG         1 1 B Y N
> C352
>       4            CAP CHIP 1.0 PF +-.25PF COG         1 1 B Y N
> C1260
>       4   2113743N07   CAP CHIP 1.5 PF +-.25PF COG       1 1 1 B Y N
> C302
>       4   2113743N10   CAP CHIP 2.2 PF +-.25PF COG       1 1 1 B Y N
> C263
>       4   2113743N12   CAP CHIP 2.7 PF +-.25PF COG       1 1 1 B Y N
> C492
>       4   2113743N16   CAP CHIP 3.9 PF +-.25PF COG       1 1 1 B Y N
> C303
>       4   2113743N18   CAP CHIP 4.7 PF +-.25PF COG       2 1 1 B Y N
> C264
>       4            CAP CHIP 4.7 PF +-.25PF COG         1 1 B Y N
> C464
>       4   2113743N19   CAP CHIP 5.1 PF + -.5PF COG       1 1 1 B Y N
> C359
>       4   2113743N20   CAP CHIP 5.6 PF + -.5PF COG       1 1 1 B Y N
> C483
>       4   2113743N24   CAP CHIP 8.2 PF + -.5PF COG       2 1 1 B Y N
> C402
>       4            CAP CHIP 8.2 PF + -.5PF COG         1 1 B Y N
> C494
>       4   2113743N26   CAP CHIP 10.0 PF 5% COG           3 1 1 B Y N
> C325
>       4            CAP CHIP 10.0 PF 5% COG             1 1 B Y N
> CNW2
>       4            CAP CHIP 10.0 PF 5% COG             1 1 B Y N
> C326
>       4   2113743N30   CAP CHIP 15.0 PF 5% COG           7 1 1 B Y N
> C450
>       4            CAP CHIP 15.0 PF 5% COG             1 1 B Y N
> C460
>       4            CAP CHIP 15.0 PF 5% COG             1 1 B Y N
> C461
>       4            CAP CHIP 15.0 PF 5% COG             1 1 B Y N
> C930
>       4            CAP CHIP 15.0 PF 5% COG             1 1 B Y N
> C931
>       4            CAP CHIP 15.0 PF 5% COG             1 1 B Y N
> C355
>       4            CAP CHIP 15.0 PF 5% COG             1 1 B Y N
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> 4 2113743N32 CAP CHIP 18.0 PF 5% COG 2 1 1 B Y N
> C1261
> 4 CAP CHIP 18.0 PF 5% COG 1 1 B Y N
> C451
> Motorola Internal Use Only
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>
> SWF3076DA Bom Report
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> LVL COMPONENT_PART DESCRIPTION QTY C Q M D P
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> 4 2113743N33 CAP CHIP 20.0 PF 5% COG 1 1 1 B Y N
> C267
> 4 2113743N34 CAP CHIP 22.0 PF 5% COG 4 1 1 B Y N
> C265
> 4 CAP CHIP 22.0 PF 5% COG 1 1 B Y N
> C408
> 4 CAP CHIP 22.0 PF 5% COG 1 1 B Y N
> C452
> 4 CAP CHIP 22.0 PF 5% COG 1 1 B Y N
> C462
> 4 CAP CHIP 22.0 PF 5% COG 1 1 1 B Y N
> C206
> 4 2113743N38 CAP CHIP 33.0 PF 5% COG 14 1 1 B Y N
> C403
> 4 CAP CHIP 33.0 PF 5% COG 1 1 B Y N
> C909
> 4 CAP CHIP 33.0 PF 5% COG 1 1 B Y N
> C910
> 4 CAP CHIP 33.0 PF 5% COG 1 1 B Y N
> C915
> 4 CAP CHIP 33.0 PF 5% COG 1 1 B Y N
> C980
> 4 CAP CHIP 33.0 PF 5% COG 1 1 B Y N
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> 4 CAP CHIP 33.0 PF 5% COG 1 1 B Y N
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> 4 CAP CHIP 33.0 PF 5% COG 1 1 B Y N
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> 4 CAP CHIP 33.0 PF 5% COG 1 1 B Y N
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> 4 CAP CHIP 33.0 PF 5% COG 1 1 B Y N
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> 4 CAP CHIP 33.0 PF 5% COG 1 1 B Y N
> C986
> 4 CAP CHIP 33.0 PF 5% COG 1 1 B Y N
> C988
> 4 CAP CHIP 33.0 PF 5% COG 1 1 B Y N
> C350
> 4 2113743N40 CAP CHIP 39.0 PF 5% COG 3 1 1 B Y N
> C962
> 4 CAP CHIP 39.0 PF 5% COG 1 1 B Y N

> C961
> 4 CAP CHIP 39.0 PF 5% COG 1 1 B Y N
> C479
> 4 2113743N42 CAP CHIP 47.0 PF 5% COG 6 1 1 B Y N
> C255
> 4 CAP CHIP 47.0 PF 5% COG 1 1 B Y N
> C256
> 4 CAP CHIP 47.0 PF 5% COG 1 1 B Y N
> C314
> 4 CAP CHIP 47.0 PF 5% COG 1 1 B Y N
> C312
> 4 CAP CHIP 47.0 PF 5% COG 1 1 B Y N
> C207
> 4 CAP CHIP 47.0 PF 5% COG 1 1 B Y N
> C203
> 4 2113743N44 CAP CHIP 56.0 PF 5% COG 1 1 1 B Y N
> C489
> 4 2113743N50 CAP CHIP 100 PF 5% COG 11 1 1 B Y N
> C1263
> 4 CAP CHIP 100 PF 5% COG 1 1 B Y N
> C262
> 4 CAP CHIP 100 PF 5% COG 1 1 B Y N
> C1264
> 4 CAP CHIP 100 PF 5% COG 1 1 B Y N
> C1265
> 4 CAP CHIP 100 PF 5% COG 1 1 B Y N
> C496
> 4 CAP CHIP 100 PF 5% COG 1 1 B Y N
> C484
> 4 CAP CHIP 100 PF 5% COG 1 1 B Y N
> C257
> 4 CAP CHIP 100 PF 5% COG 1 1 B Y N
> C306
> 4 CAP CHIP 100 PF 5% COG 1 1 B Y N
> C204
> 4 CAP CHIP 100 PF 5% COG 1 1 B Y N
> C468
> 4 CAP CHIP 100 PF 5% COG 1 1 B Y N
> C115
> 4 2113743N69 CAP CHIP 1.8PF 16V +/-.25PF 1 1 1 B Y N
> C1262
> 4 2113928J08 CAP CERAMIC CHIP 10.0UF 1 1 1 B Y N
> C942
> 4 2113928P04 CAP CER CHIP 1.0UF 20% 6.3V 2 1 1 B Y N
> C987
> 4 CAP CER CHIP 1.0UF 20% 6.3V 1 1 B Y N
> C703
> 4 2311049A56 CAP TAN CHIP A/P 4.7 20 10 4 1 1 B Y N
> C913
> 4 CAP TAN CHIP A/P 4.7 20 10 1 1 B Y N
> C928
> 4 CAP TAN CHIP A/P 4.7 20 10 1 1 B Y N
> C929
> 4 CAP TAN CHIP A/P 4.7 20 10 1 1 B Y N
> C940
> 4 2311049A89 CAP TANT CHIP 22 UF 4V 10% 1 1 1 B Y N

> C960
> 4 2409134J27 IND CHIP FER FLTR 1000 0402 1 1 1 B Y N
> L351
> 4 2409154M07 IND CER MLTILYR 3.3NH 1005 1 1 1 B Y N
> L451
> 4 2409154M10 IND CER MLTILYR 5.6NH 1005 1 1 1 B Y N
> L263
> 4 2409154M14 IND CER MLTILYR 12.0NH 1005 1 1 1 B Y N
> L1255
> 4 2409154M31 IND CER MLTILYR 3.9NH 1005 3 1 1 B Y N
> L450
> 4 IND CER MLTILYR 3.9NH 1005 1 1 B Y N
> L478
> 4 IND CER MLTILYR 3.9NH 1005 1 1 B Y N
> L256
> 4 2409154M35 IND CER MLTILYR 8.2NH 1005 1 1 1 B Y N
> L461
> 4 2409154M37 IND CER MLTILYR 12.0NH 1005 1 1 1 B Y N
> L460
> 4 2409154M81 IND CER MLTILYR 2.7 NH 1005 1 1 1 B Y N
> L481
> 4 2409154M88 IND CER MLTILYR 10.0NH 1005 3 1 1 B Y N
> L350
> Motorola Internal Use Only
>
>
> SWF3076DA Bom Report
>
> LVL COMPONENT_PART DESCRIPTION QTY C Q M D P
> REF
> ---------- ---------- ---------- ---- - - - - -
> ------
> 4 2409154M88 IND CER MLTILYR 10.0NH 1005 3 1 1 B Y N
> L353
> 4 IND CER MLTILYR 10.0NH 1005 1 1 B Y N
> L322
> 4 2409154M95 IND CER MLTILYR 39.0NH 1005 2 1 1 B Y N
> L254
> 4 IND CER MLTILYR 39.0NH 1005 1 1 B Y N
> R256
> 4 2409350L15 IND CER LZRETCH 22 NH 2 1608 1 1 1 B Y N
> L255
> 4 2409377M01 IND CHIP WW 1.8 NH 10% 1608 1 1 1 B Y N
> L250
> 4 2409646M13 IND CER MULTILYR 39NH 1608 1 1 1 B Y N
> L960
> 4 2409646M45 IN CER MULTILYR 1 1 1 B Y N
> L475
> 4 2409646M76 IN CER MULTILYR 3.9NH 1608 1 1 1 B Y N
> CR105
> 4 2409646M85 IN CER MULTILYR 22 NH 1608 1 1 1 B Y N
> C109
> 4 2409646M86 IN CER MULTILYR 27 NH 1608 3 1 1 B Y N
> L479
> 4 IN CER MULTILYR 27 NH 1608 1 1 B Y N
> L490

```
>       4             IN CER MULTILYR 27 NH 1608          1 1 B Y N
> L101
>       4   2409646M94   IND CER MULTILYR 47NH 1608        1 1 1 B Y N
> L482
>       4   2462587Q66   IND CHIP 100,000 NH 10%           2 1 1 B Y N
> L201
>       4             IND CHIP 100,000 NH 10%             1 1 B Y N
> L202
>       4   2602538T01   TEMP 2603862K03 VCOSHLD 1.98MM    1 1 1 B Y N
>
>       4   2603863K02   SHIELD TX & RX                    1 1 1 B Y N
> SH300
>       4   2604991Z03   SHIELD LOGIC                     1 1 1 B Y N
> SH700
>       4   2809329U02   PLUG INTRBD 14PIN .5MM SMD       1 1 1 B Y N
> J800
>       4   3903746K01   CNTCT ANT UPPER                  1 1 1 B Y N
> A1
>       4   4009368L03   SW TACTILE RT ANGL 3 POLE SMD     3 1 1 B Y N
> DWN
>       4             SW TACTILE RT ANGL 3 POLE SMD       1 1 B Y N
> SMART
>       4             SW TACTILE RT ANGL 3 POLE SMD       1 1 B Y N
> UP
>       4   4802536T01   TEMP 4809283D24 SCREENED          1 4 1 B Y N
> U250
>       4   4802536T02   TEMP 4809283D24 SCRND 1.98MM      1 1 1 B Y N
>
>       4   4809283D33   OSC MOD VCO 1785MHZ 8X9MM SMD     1 4 1 B Y N
> U250
>       4   4809527E24   TSTR NPN RF MRF949LT1 SC-90       6 1 1 B Y N
> Q253
>       4             TSTR NPN RF MRF949LT1 SC-90         1 1 B Y N
> Q255
>       4             TSTR NPN RF MRF949LT1 SC-90         1 1 B Y N
> Q262
>       4             TSTR NPN RF MRF949LT1 SC-90         1 1 B Y N
> Q455
>       4             TSTR NPN RF MRF949LT1 SC-90         1 1 B Y N
> Q300
>       4             TSTR NPN RF MRF949LT1 SC-90         1 1 B Y N
> Q400
>       4   4809527E30   TSTR NPN RF NE68719 SC90          2 1 1 B Y N
> Q461
>       4             TSTR NPN RF NE68719 SC90            1 1 B Y N
> Q490
>       4   4809527E32   TSTR NPN RF BFP320W              1 1 1 B Y N
> Q451
>       4   4809579E02   TSTR MOSFET N-CHAN 25K1830       1 1 1 B Y N
> Q921
>       4   4809579E29   TSTR FET P-CHAN SI3443DV 6TSOP    2 1 1 B Y N
> Q932
>       4             TSTR FET P-CHAN SI3443DV 6TSOP      1 1 B Y N
> Q938
>       4   4809579E39   TSTR FET DUAL FDG6323L SC70-6     2 1 1 B Y N
> Q00920
```

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>        4              TSTR FET DUAL FDG6323L SC70-6       1 1 B Y N
> Q00939
>        4   4809606E08   DIODE DUAL SCHOTTKEY RB715F       1 1 1 B Y N
> CR701
>        4   4809608E03   TSTR DIG PNP DTA114YE             3 1 1 B Y N
> Q981
>        4              TSTR DIG PNP DTA114YE               1 1 B Y N
> Q106
>        4              TSTR DIG PNP DTA114YE               1 1 B Y N
> Q345
>        4   4809653F07   RECT SCHTTKY 1A MBRM120ET3        1 1 1 B Y N
> CR932
>        4   4809877C13   DIODE VARACTOR ISV305 SMD         1 1 1 B Y N
> CR0250
>        4   4809939C03   TSTR DUAL NPN/PNP UMH3            2 1 1 B Y N
> Q105
>        4              TSTR DUAL NPN/PNP UMH3              1 1 B Y N
> Q104
>        4   4809939C04   TSTR DUAL PNP/NPN UMC3            1 1 1 B Y N
> Q634
>        4   4809939C05   TSTR DUAL NPN/PNP UMH 5           2 1 1 B Y N
> Q344
>        4              TSTR DUAL NPN/PNP UMH 5             1 1 B Y N
> Q346
>        4   4809939C08   TSTR DUAL PNP/PNP UMA6NTL         2 1 1 B Y N
> Q101
>        4              TSTR DUAL PNP/PNP UMA6NTL           1 1 B Y N
> Q102
>        4   4809939C28   TSTR DUAL NPN/NPN UPA807T         1 1 1 B Y N
> Q1254
>        4   4809948D12   DIODE PIN BAR63-02W ESC           2 1 1 B Y N
> CR300
>        4              DIODE PIN BAR63-02W ESC             1 1 B Y N
> CR301
>        4   4809948D13   DIODE RF SWITCH BA892 ESC         2 1 1 B Y N
> CR251
>        4              DIODE RF SWITCH BA892 ESC           1 1 B Y N
> CR307
>        4   4809948D16   DIODE QUAL TVS 12V SMS12 SOT23    1 1 1 B Y N
> VS0945
>        4   4809948D30   DIODE PIN BAR64-02W SCD-80        1 1 1 B Y N
> CR306
>                    Motorola Internal Use Only
>
>
>                      SWF3076DA Bom Report
>
>       LVL COMPONENT_PART  DESCRIPTION                    QTY C Q M D P
> REF
> ---------- --------------- ------------------------------ ---- - - - - -
> ------
>        4   4809995L05   XTAL QUARTZ 32.768KHZ CC4V-T1     1 1 1 B Y N
> Y900
>        4   5085838G01   SPKR ALERT EM 2.5V 8.5MM SMD      1 1 1 B Y N
> AL900
>        4   5102500T03   5199366A01 .16 PROG FLASH KRMR    1 1 1 B Y N
```

> U701
> 5 5199366A01 IC FLASH ROM 16M 28F160B3B X16 1 1 1 B Y N
>
> 4 5109509A16 IC SRAM 64KX16 KM616FS1000 BGA 1 1 1 B Y N
> U702
> 4 5109522E14 IC 2-INPUT OR GATE TC7S32FU 1 1 1 B Y N
> U703
> 4 5109731C23 IC OP AMP DUAL LMV822 8SOP 1 1 1 B Y N
> U980
> 4 5109879E26 IC CUST GCAP 2 PASS 4 100 BGA 1 1 1 B Y N
> U900
> 4 5109908K38 IC RFPA GAAS SINGL BND EN249 1 1 1 B Y N
> U400
> 4 5109908K39 IC RFPA GAAS DUAL BND EN249 1 4 1 B Y N
> U300
> 4 5109908K46 IC RFPA GAAS 3.5W EN252 DCS 1 1 1 B Y N
> U300
> 4 5199406C03 IC DSP MARK WHITECAP 179 GBA 1 1 1 B Y N
> U700
> 4 8485957H12 PCB GSM KRAMER 1 1 1 B Y N
> PCB
> 4 9103769S01 FLTR CER LCBP 1.8GHZ 3225 SMD 1 1 1 B Y N
> FL465
> 4 9109069E01 FLTR SAW 1842MHZ SMD 1 1 1 B Y N
> FL0450
> 4 9109450C02 FLTR SAW BP 925-960 MHZ SMD 1 1 1 B Y N
> FL460
> 4 9109450C03 FLTR SAW BP 925-960 MHZ SMD 1 1 1 B Y N
> FL470
> 4 9109487U01 FLTR SAW BP 400MHZ SMD 1 1 1 B Y N
> FL457
> 4 9185906G03 FLTR CER DIPLEX MCIC 16BGA 1 1 1 B Y N
> FL0300
> 2 SYN6939A STARTAC 210 KYBD 1 1 1 M Y N
>
> 3 0109037A93 KYBD STAC210 TOP SIDE 1 1 1 M Y Y
>
> 4 0609591M12 RES CHIP DUAL 82 5% 0.63W 3 1 1 B Y N
> R00970
> 4 RES CHIP DUAL 82 5% 0.63W 1 1 B Y N
> R00971
> 4 RES CHIP DUAL 82 5% 0.63W 1 1 B Y N
> R00972
> 4 0909328U02 RECPT INTRBD 14PIN .5MM SMD 1 1 1 B Y N
> J00800
> 4 4009307U01 SW REED 5.8X1.9MM LEADED 1 1 1 B Y N
> S00920
> 3 0109037A94 KYBD STAC210 BOT SIDE 1 1 1 M Y Y
>
> 4 4809496B12 LED CHIP GRN 1608 LNJ314G8 6 1 1 B Y N
> DS0970
> 4 LED CHIP GRN 1608 LNJ314G8 1 1 B Y N
> DS0971
> 4 LED CHIP GRN 1608 LNJ314G8 1 1 B Y N
> DS0972
> 4 LED CHIP GRN 1608 LNJ314G8 1 1 B Y N

> DS0973
> 4 LED CHIP GRN 1608 LNJ314G8 1 1 B Y N
> DS0974
> 4 LED CHIP GRN 1608 LNJ314G8 1 1 B Y N
> DS0975
> 4 8404564Z01 PCB KRAMER KYPD 1 1 1 B Y N
>
> 3 1185715J01 ADHESIVE KYBRD KRAMER 1 1 1 B Y N
>
> 3 4004877Z02 SW ARRAY SNAP DOMES 19P 1 1 1 B Y N

MOTOROLA

Mechanical Spare Parts List

GSM Kramer - V3688

Version 1.7

21st Aug 1999

Xcvr Item Number		SWF3076PD	SWF0387AA	SWF0379AA	SWF0381AA	SWF0380AA
Product	-	Kramer	Kramer	Kramer	Kramer	Kramer
Additional Info	-	StarTAC 210	STAGE II	STAGE II	STAGE II	STAGE II
Colour	-	Black	Black	Radar Blue	Galaxy Grey	Light Titanium
Make	-	Motorola	Motorola	Motorola	Motorola	Motorola
System	-	GSM	GSM	GSM	GSM	GSM
Spare Xcvr Number	-	SE0044DB1Z1	SE0725AB1B1	SE0725AP3B1	SE0725AP3B1	SE0725AQ3B1
Spare PCB Number	-	Not Available	Not Available	Not Available	Not Available	Not Available
Frnt Hsng Assy	-	SYN7911A	SYN8162A	SYN8164A	SYN8165A	SYN8161A
..Assy Frnt Hsng	-	0104792Z01	0104792Z01	0104792Z03	0104792Z02	0104792Z04
..Hinge Mechanism	-	5504765Z05	5504765Z05	5504765Z05	5504765Z05	5504765Z05
..Speaker Earpc 15mm	-	5003880S01	5003880S01	5003880S01	5003880S01	5003880S01
..Batt Li 3.3v Coin Cell	-	6003710K04	6003710K04	6003710K04	6003710K04	6003710K04
..LCD Display 96x54	-	7203908S05	7203908S06	7203908S06	7203908S06	7203908S06
..Pad Kramer	-	7585766G01	7585766G01	7585766G01	7585766G01	7585766G01
..Assy Flip Rear	-	0185895H01	0185895H02	0185779K03	0185779K02	0185779K02
..Assy Flip Frnt	-	0185896H01	0185896H02	0185778K03	0185778K02	0185778K02
..Pad Flip	-	7585719J01	7585719J01	7585719J01	7585719J01	7585719J01
Lens Tape	-	1109284E01	1109284E01	1109284E01	1109284E01	1109284E01
Lens	-	6185833G02	6185833G02	6185833G02	6185833G02	6185833G02
Rear Hsng Assy	-	0104793Z02	0104793Z02	0104793Z04	0104793Z03	0104793Z05
..Screw Internal Frnt Crick	-	0309147T03	0309147T03	0309147T03	0309147T03	0309147T03
..Rear Hsng Plastic	-	1503853K01	1503853K02	1503853K04	1503853K03	1503853K03
..Button Voice	-	3809440U01	3809440U01	3809440U01	3809440U01	3809440U01
..Spring Mechanical Con	-	4104539Z01	4104539Z01	4104539Z01	4104539Z01	4104539Z01
..Spring Compressions	-	4109378U01	4109378U01	4109378U01	4109378U01	4109378U01
..Clip Vibrator Bracket	-	4285952G03	4285952G03	4285952G03	4285952G03	4285952G03
..Clip Vibrator Contact	-	4285953G05	4285953G05	4285953G05	4285953G05	4285953G05
..Latch Battery	-	5509377U01	5509377U01	5509377U01	5509377U01	5509377U01
..Motor Vibrator 6mm	-	5909382K01	5909382K01	5909382K01	5909382K01	5909382K01
H&H Parts	-	SHN6861A	SHN6861B	SHN6861B	SHN6861B	SHN6861B
..Stubby Antenna	-	0185829G02	0185829G02	0185829G02	0185829G02	0185829G02
..Grommet Microphone	-	0585699J01	0585699J01	0585699J01	0585699J01	0585699J01
..Keypad	-	3809378T02	3809378T08	3809378T08	3809378T08	3809378T08
..Antenna Insert	-	4385988H02	4385988H02	4385988H02	4385988H02	4385988H02
..Mic 6mm	-	5009135L07	5009135L07	5009135L07	5009135L07	5009135L07
..Light Guide	-	6185635H02	6185635H02	6185635H02	6185635H02	6185635H02
..Pad Connector	-	7585824J01	7585824J01	7585824J01	7585824J01	7585824J01
Keyboard	-	SYN6939B	SYN8103A	SYN8103A	SYN8103A	SYN8103A
..Adhesive Kybrd	-	1185715J01	1185715J01	1185715J01	1185715J01	1185715J01
..SW Array Domes	-	4004877Z02	4004877Z03	4004877Z03	4004877Z03	4004877Z03
Slim Hsng Door Cover	-	SYN7117B	SYN7117B	SYN8111A	SYN8110A	SYN8112A
Thick Hsng Door Cover	-	SYN7118A	Not Available	Not Available	Not Available	Not Available

Internal Eschuteon	Orange	5403797S24
	TIM	5403797S03
	Omnitel	5403797S04
	Wind Italy	5403797S05
	Motorola	5403797S07
	Telefonica	5403797S10
	Amena	5403797S13
	One to One	5403797S17
	Airtel	5403797S11

Parts Not Available

Part Number has changed

DUALBAND KRAMER H13

DSM KRAMER TRANCEIVER
P/N: 8480815613
SHEET 1 (LOGIC)

REV.	COMMENTS	DATE
P1_-1	COPIED FROM 8480815701	06/05/97
P1	RF RELEASE	10/28/97
P1_-35	P1 RELEASE	11/25/97
P2_-36	RELEASED FOR PROTOTYPE	02/05/98
P3_-22	RELEASED FOR PROTOTYPE	04/06/98
P4_-27	RELEASED FOR PROTOTYPE	05/25/98
P4.1_-3	RELEASED FOR PROTOTYPE	06/26/98
P4.1_-5	VALUE CHANGES	07/14/98
P4.1_-5	VALUE CHANGES	07/15/98
P4.2	RELEASED FOR PROTOTYPE	07/22/98
P4.3	RELEASED FOR PROTOTYPE	07/28/98
P5	RELEASED FOR PROTOTYPE	08/12/98
P5.1	RELEASED FOR PROTOTYPE	08/28/98
P5.2	RELEASED FOR PROTOTYPE	09/04/98
P6	RELEASED FOR PROTOTYPE	09/21/98
P7	RELEASED FOR PROTOTYPE	10/05/98
P7.1	RELEASED FOR PROTOTYPE	10/12/98
P7.2	RELEASED FOR PROTOTYPE	10/13/98
P7.3	RELEASED FOR PROTOTYPE	10/25/98
P8	RELEASED FOR PROTOTYPE	10/30/98
P9	RELEASED FOR PROTOTYPE	11/02/98
P10	RELEASED FOR PROTOTYPE	11/05/98
P11	RELEASED FOR PROTOTYPE	11/09/98
P12	RELEASED FOR PROTOTYPE	11/13/98
P13	RELEASED FOR PROTOTYPE	11/20/98

REVISIONS

GSM SERVICE SUPPORT GROUP	04.10.99
LEVEL 3 AL SCHEMATICS	Rev. 1.0
DUAL BAND KRAMER	
Michael Hansen, Ray Collins, Ralf Lorenzen	Page 2of 3

Dual Band KRAMER P11

WHITECAP

U700
WHITE_CAP

GCAP II

U900
GCGAP_II

CHARGER / SOURCE SELECT

- 5V REG.

KEYBOARD

SIM CON.

VIBRA CON.

J700 FLIP CON.

J600 EXT CON.

U701 EPROM EEPROM

U702 SRAM

J650

MIC CON

U980

U981

U901

U801

Q710

Q803

Q911

Q912

Q921

Q920

Q960

Q901

Q902

Q932

Q942

Q634

Q635

Q938

Q939

Q950

Q805

Q806

CR942

CR701

CR910

CR931

CR932

CR940

CR920

CR948

VS944

VS945

Y900
32.768kHz

AL900

U950

J810

J811

GSM Service Support
Level 3 Authorized

RX SIGNAL PATH
TX SIGNAL PATH
MAIN VCO SIGNAL PATH
TUNING VOLTAGES
13 MHz REFERENCE CLOCK
DATA BUS
ADDRESS BUS
TEXT REFERENCE SIGNALS

GSM KRAMER TRANSCEIVER
P/N: 84M0070401
SHEET 1 (L0202)

ISS.	COMMENTS	DATE
P1.1	COPIED FROM 84M0070101	06-05-97
P1	RF RELEASE	10-28-97
P1.35	P1 RELEASE	11-25-97
P2.36	RELEASED FOR PROTOTYPE	02-03-98
P3.02	RELEASED FOR PROTOTYPE	04-06-98
P4.27	RELEASED FOR PROTOTYPE	05-25-98
P4.5.1	RELEASED FOR PROTOTYPE	06-30-98
P4.5.2	VALUE CHANGES	07-14-98
P4.5.3	VALUE CHANGES	07-15-98
P4.4	RELEASED FOR PROTOTYPE	07-22-98
P4.3	RELEASED FOR PROTOTYPE	07-28-98
P5	RELEASED FOR PROTOTYPE	08-12-98
P5.1	RELEASED FOR PROTOTYPE	08-28-98
P5.2	RELEASED FOR PROTOTYPE	09-04-98
P6	RELEASED FOR PROTOTYPE	09-21-98
P7	RELEASED FOR PROTOTYPE	10-05-98
P7.1	RELEASED FOR PROTOTYPE	10-12-98
P7.2	RELEASED FOR PROTOTYPE	10-15-98
P7.3	RELEASED FOR PROTOTYPE	10-26-98
P8	RELEASED FOR PROTOTYPE	10-30-98
P9	RELEASED FOR PROTOTYPE	11-02-98
P10	RELEASED FOR PROTOTYPE	11-04-98
P11	RELEASED FOR PROTOTYPE	11-06-98

REVISIONS

GSM SERVICE SUPPORT GROUP	01.10.99
LEVEL 3 COLOUR SCHEMATICS	Rev. 1.0
GSM KRAMER Audio Logic	
Ralf Lorenzen, Ray Collins, Michael Hansen	Page 3of 3